Electromigration Characteristics of Copper Damascene Interconnects Integrated with SiLK*, Low k- Dielectric

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Abstract:

The reduction of the product of Resistance times Capacitance is minimizing the interconnect impact on the circuit delay. To reduce the resistance, copper has been used as the conductor for the VLSI interconnects. To reduce the capacitance, SiLK* semiconductor dielectric is used as an interlevel dielectric. In this paper, we will discuss the electromigration characteristics of copper interconnects encapsulated by SiLK resin, a low k- dielectric. The Cu interconnects were fabricated used a dual damascene process and electro-plating (EP). The test structures were stressed at a temperature T = 295) C and the stress current density was J_{stress} = 10.0 mA /um^2. The Interlevel Dielectric (ILD) was composed of a composite layer, including SiLK* dielectric. The electromigration stress testings were performed in four (4) electron flow directions, CA-M1, V1-M1, V1-M2 and V2-M2 to complete the evaluation of the electromigration characteristics of the dual damascene process of M1 and M2 interconnects. The stress results of the electromigration life times of copper in SiLK as ILD showed no degradation compared to copper and silicon dioxide.

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* SiLK is a trade mark of the Dow Chem. Co.