The Impact of Wafer-Level Layer Transfer on High Performance Devices and Circuits for 3D IC Fabrication

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Three dimensional (3D) integrated circuits (ICs) have the potential to dramatically enhance chip performance, functionality, and device packing density. They also promise to create new opportunities for microchip architecture and may facilitate the integration of heterogeneous materials, devices, and signals. Yet to realize these potential advantages, the processes required to build circuits with multiple layers of active devices must be compatible with high performance technologies. We introduce a new scheme for building 3D ICs based on the layer transfer of functional circuits. The key to this transfer is a wafer-level bonding approach that joins high performance device layers fabricated by conventional means. We demonstrate that the processes required for stacking active device layers can preserve the electrical integrity of short-channel silicon metal oxide semiconductor field effect transistors (MOSFETs) and ring oscillator circuits. The wafer-level layer transfer technique uses only low process temperatures and minimizes mechanical stresses to preserve the sensitive devices on 200 mm diameter silicon wafers. We show that state-of-the-art 130 nm silicon-on-insulator (SOI) devices with copper metallization and low-k inter-level dielectric insulators can withstand the transfer processes, with virtually no change in the intrinsic device characteristics. This result is an essential step toward successful realization of high performance 3D ICs.