Wafer Bonding and Thinning Integrity for 3D-IC Fabrication

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Wafer scale three-dimensional (3D) integration is recognized as an emerging technology to increase the performance and functionality of integrated circuits (ICs). In our approach, fully processed wafers are aligned and bonded with dielectric glues, followed by top wafer thinning to less than 10 µm. The IC back end bonding and thinning processes are fully compatible with semiconductor processing protocols. Subsequently, inter-wafer interconnects are formed using a copper damascene patterning process [1-3]. The wafer bonding and thinning integrity are presented in this paper.

The bonded wafers should have high bond strength and low interfacial stress in order to resist the impacts of subsequent processing steps; *i.e.*, mechanical thinning, CMP (chemical-mechanical planarization), and thermal cycling. Several low-k dielectric polymers including benzocylcobutene (BCB) and poly arylene ether (Flare) have been used as the bonding glue. The fraction of bonded area has been examined by optical inspection and the bonding strength between the glue and the contiguous layer has been quantified by four-point bending test. This test measures load plateau under displacement rate control [4]. The load plateau is obtained while a crack propagates along the interface being studied. Figure 1 represents the schematic illustration of four point bending specimen before and after bending; Figure 2 shows load-displacement curve, which depicts the load plateau. A baseline 200 mm wafer bonding process has been established for BCB and Flare as dielectric glue materials. A high interfacial adhesion energy is obtained, *e.g.*, ~8 J/m^2 using BCB with a thickness of ~2.6 µm and ~18 J/m^2 using Flare with a thickness of ~0.6 µm for a silicon wafer bonded to a TCE-matched glass wafer (done for optical inspection). Interfacial adhesion energy between BCB and PECVD oxide for a bonded pair of silicon wafers with PECVD oxide was ~31 J/m^2, and that between BCB and thermal oxide was ~34 J/m^2. While large areas of void-free bonding can be achieved using Flare, complete void-free bonding is routinely obtained across 200mm wafers using BCB.

Subsequent to wafer bonding, thinning processes for bonded pairs of blanket wafers (bulk silicon, SOI, etch-stop silicon, CTE-matched glass), and processed wafers (*e.g.*, with interconnect test structures) have been evaluated. No visible changes at the bonding interface can be observed after the silicon substrates are thinned to ~30 µm by backgrinding and polishing. A wafer having multi-level copper interconnect test structures (provided by International SEMATECH) was bonded with BCB to a TCE-matched glass wafer. No changes could be visually observed after the mechanical thinning of the silicon substrate to ~35 µm (see Figure 3). Electrical tests on such wafers show a very slight change in the via resistance and a change of one order of magnitude in comb-to-comb leakage current after two bonding and thinning processes. Though these results are very promising, thinning failure in some cases occurs at a nominal thickness of ~15 µm. These failures have a distinct pattern, attributed to the process non-uniformities and/or wafer defects.

This paper discusses the following effects on the bonding integrity and their impact on the mechanical thinning process: (1) glue thickness, (2) glue film preparation (*e.g.*, adhesion promoters and surface treatments), (3) heat treatment during bonding (*e.g.*, final curing temperature and bonding temperature/pressure as a function of time), and (4) material on wafer surface (*e.g.*, silicon, silicon oxides, silicon nitride, glasses and metals). Fortification of the bonding strength by changes of interfacial chemistry through glue film preparation, heat treatment, and glue contacting materials under the thinned glue thickness will be discussed. Failure mechanisms of the thinning process and its effect on the characteristics of the processed wafers (with passive and active devices) will be addressed.

References:

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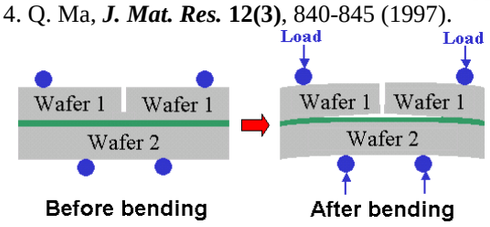

Figure 1. Schematic of four point bending specimen before and after bending.

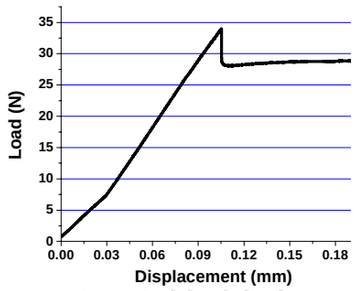

Figure 2. Typical load-displacement curve of four point bending test.

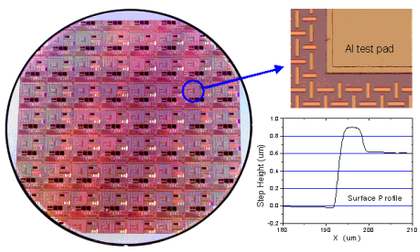

Figure 3. Wafer bonding/thinning result for a SEMATECH wafer with multi-level Cu-interconnects (provided by International SEMATECH) bonded on a glass wafer. This was observed after the mechanical thinning of the silicon substrate to ~35 µm and photo was taken through the glass wafer.