3D-INTEGRATION OF INTEGRATED CIRCUITS BY INTERCHIP VIAS (ICV) AND CU/SN SOLID LIQUID INTERDIFFUSION (SOLID)

P. Ramm *, A. Klumpp, R. Wieland

Fraunhofer Institute IZM, Munich
Hansastrasse 27d, 80686 Muenchen

Phone: * 0049 89 54759 539
Fax: 0049 89 54759 100
E-Mail: ramm@izm-m.fhg.de

ABSTRACT

The tungsten-based InterChip Via (ICV) technology was evaluated as a fully CMOS-compatible wafer-scale process for Vertical System Integration VSI®, that provides vertical electrical interchip interconnects placed at arbitrary locations, without intervention to the IC´s fabrication technologies. The mechanical connection between top and bottom wafer is performed by a thin polyimide layer. The electrical interconnects are performed after bonding of the wafers. This approach is already reported elsewhere.
Our new approach combines the best processes from the interchip via process sequence and the solid liquid interdiffusion (SOLID) between copper and tin to have instant mechanical and electrical connection of the stacked wafers.
The interchip vias are prepared on the top wafer by etching through all dielectric layers, followed by a typically 12 µm deep silicon trench etch. For lateral via isolation, a dielectric spacer technique is applied using highly conformal CVD of O3/TEOS-oxide. After a TiN deposition (20 nm MOCVD TiN using 8 cycles of TDMAT pyrolysis and N2/H2 plasma densification) the interchip vias are metallized by using MOCVD of tungsten. The tungsten deposition process provides excellent step coverage. After via fill the W/TiN is etched back using a fluorine based high density plasma process at elevated temperatures.
The lateral electrical connection of the metallized interchip vias with the metal level of the top wafer is done by opening contact windows on the top wafer followed by a standard metallization. The top wafer is then adhesively bonded to a handling wafer and thinned with high uniformity until the interchip vias are opened from the rear (fig. 2). After deposition of dielectric layers for electrical isolation and opening to the interchip vias, the copper for SOLID stacking is deposited. The bottom wafer is planarised and coated with structured solid metal (tin). The stabilized top wafer and the bottom wafer are then optically adjusted and stacked. After bonding at approximately 300 °C, the handling wafer is removed, leaving the desired wafer stack that can be further processed like a standard silicon wafer in a CMOS line.
Finally, the bond pads are opened and the 3D-integrated devices can be tested, separated and mounted by use of standard procedures. The sketch in figure 1 shows thinned top wafer with interchip via and the solid liquid interdiffusion metals on the backside (copper). The bottom wafer carries the mirror designed SOLID-metal tin.

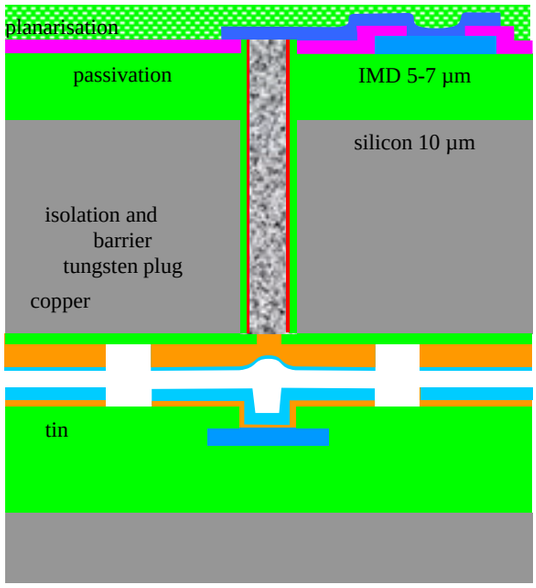

Fig. 1: ICV / Solid Liquid Interdiffusion for 3D-Integration

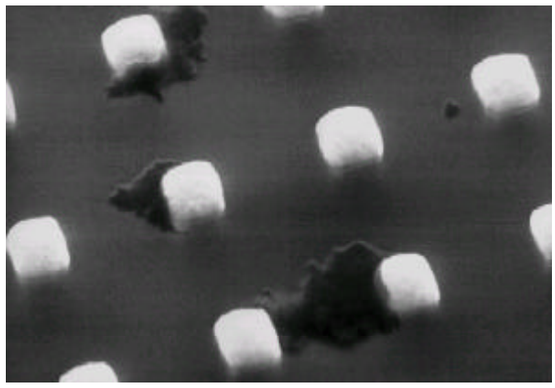

Fig. 2: Opened interchip tungsten vias from the rear of the thinned top wafer.
The designed ICV-dimensions at the front side of the top wafer are 2.0 x 2.0 µm^2