3D System-on-a-Chip using Dielectric Glue Bonding and Cu Damascene Inter-Wafer Interconnects

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This paper presents a technology platform of three-dimensional system-on-a-chip (3D SoC) – an emerging technology to alleviate the interconnect limitations of Cu/low-k and processing and material limitations of current 2D SoCs. Our monolithic wafer-level 3D SoC approach uses wafer bonding with dielectric glues and Cu damascene inter-wafer interconnects. Four major processing steps, i.e., wafer alignment, wafer bonding, wafer thinning, and inter-wafer interconnection (high-aspect-ratio via etch and fill) are delineated and characterized using a test vehicle of 3D via-chain structures. A viable baseline process flow that accounts for the capabilities and limitations of the various process steps is described. This 3D SoC technology platform offers the potential for future low-cost, highly integrated CMOS-based systems with very high performance, functionality and packaging density. It can also be extended to 3D SoCs for opto-electronic, bio-molecular and other micro/nano heterogeneous system applications. Detailed approach, experimental results and discussions will be presented at the conference.

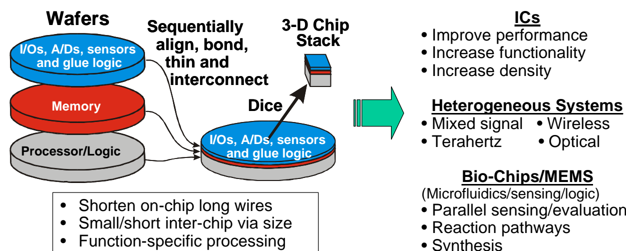

Fig. 1. Schematic of a 3D SoC concept, formed by monolithic wafer alignment, bonding, thinning and inter-wafer interconnection.

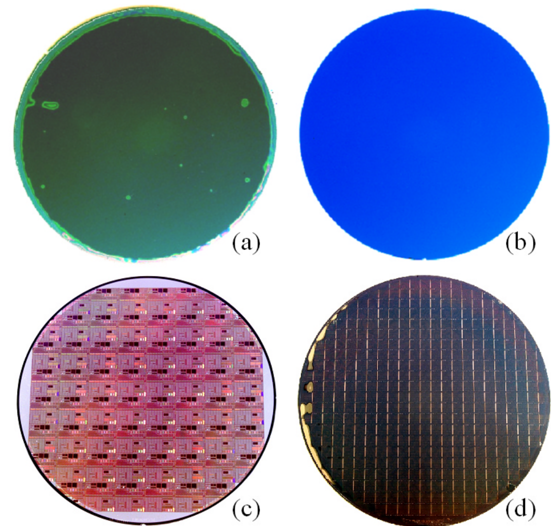

Fig. 2. Wafer bonding results: (a) Corning glass 7740 bonded to Prime Si with Flare, (b) PG&O glass 1737 bonded to Prime Si with BCB, (c) PG&O glass 1737 bonded to a SEMATECH wafer with multi-level Cu-interconnects (provided by International SEMATECH, and (d) two via-chain patterned wafers bonded with BCB. No visible changes can be observed after Si wafers are thinned mechanically (grinding/polishing) to ~ 30 μm.

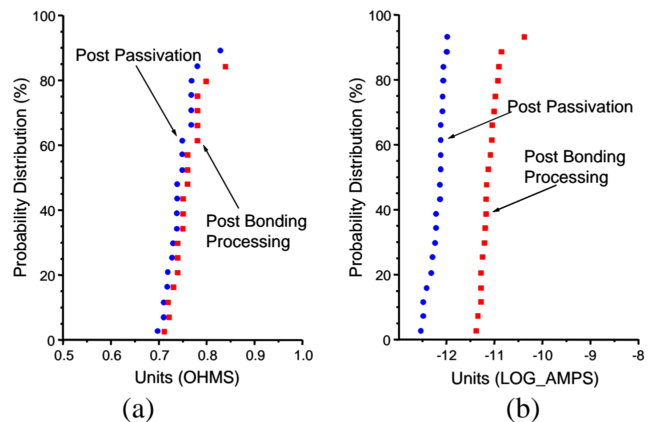

Fig. 3. Electrical tests of SEMATECH wafer before and after wafer bonding, thinning, and BCB glue removal processes. (a) Probability chart of 360k 0.25 μm via chain resistance. (b) Probability chart of comb-to-comb bridging current at 5V. Data provided by International SEMATECH.