Modeling of Thermal Dynamics and Mechanical Stress in 3D-IC Structure

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High-performance face-to-face chip stacking is being developed to interconnect two integrated circuits. The wafers are aligned, and then bonded face-to-face using a thin layer of dielectric glue. The top wafer is backside thinned to a few microns, using one of several techniques. Then reasonably short, but fairly high aspect ratio copper vias through the backside of thinned wafer are fabricated to provide vertical interconnection between two wafers. However, severe thermal stresses could well be induced in the multi-layered wafer stacks during subsequent processing of the bonded wafers, as a result of mismatch of thermal expansion of interconnect materials. These stresses may cause pre-mature failure of the interconnections and system failure.

This paper discusses the inter-wafer via stresses induced during a worst-case scenario of wafer processing. In a chamber, a wafer stack consisting two 200mm bonded wafers is suddenly heated from either upper or lower surfaces. The finite element method was used to study transient thermal-mechanical response of the wafer stack shown in Fig. 1. The copper is modeled as an elasto-purely plastic material [2], and the BCB glue is regarded as an elasto-plastic material multi-linear hardening. Two failure mechanisms for the vias were considered: plastic yielding and void growth. The corresponding failure criteria are thus given by $\sigma_e < \sigma_Y$ and $\sigma_m < \sigma_{cavitation}$, where σ_e and σ_m are the Von Mises and mean stresses, and σ_Y and $\sigma_{cavitation}$ are the yield and cavitation stresses [1], respectively. Four inter-wafer vias are explicitly included in the simulation to date.

Fig.2 shows the evolution of transient temperature difference between several points and the heated surface when the processing temperature is 400°C. In the case of heating from the thinned wafer surface, i.e. T_s = 400°C, the temperature of the points in the metal layers are almost equal due to the high thermal conductivity of the copper via. However, the temperature differences at point g in the glue layer are much higher during the initial period (t < 64 μsec.) of heat conduction as result of the very low thermal conductivity and diffusivity. Therefore, the BCB glue serves as an insulation layer, while the inter-wafer vias provide additional pathways to heat conduction.

The results of stress and strain for the 1μm vias show that the vias yield and plastic strains accumulate as the processing temperature is held at 400°C. Further analysis shows that the thermal expansion of BCB glue in the *y*-direction can cause yielding of the vias due to the large axial tension. The yielding temperatures of the inter-wafer vias can be determined by the transient BCB glue temperatures when the vias start to yield, as indicated by point A and B in Fig. 2. This worst-case scenario model predicts that the critical processing temperature for the via below the yielding point is about 115°C. The via density effect on the stress field of inter-wafer vias of 1 μm in diameter (d) were examined by employing two distinct via spacing: 14d and 4d below the yielding temperature. While the vias do not yield, voids may grow as the local original defect density exceeds a critical value [1]. The maximum values of Von Mises stress and mean stress in the vias decrease as the via density increases as result of the reduction of average tensile stress in each via. The via size effect was verified using via diameters of 1, 5 and 10 μm. As expected, the stresses are reduced as the via size increases.

We conclude that the larger CTE for BCB relative to that of Cu can cause large stresses to build up in the inter-wafer vias. Our simple model indicates that for small enough vias, this could lead to reliability problems.

References

[1] Huang, Y., 1996, "A model study of thermal stress-induced voiding in electronic packaging," *Journal of Electronic Packaging*, Vol. 118, p.229.

[2] Runnels, S.R., et al., 2002, "Advanced Experimental and Computational Tools for Robust Evaluation of On-chip Interconnect Reliability", *IEEE Transactions on Semiconductor Manufacturing*, Vol. 15(3), pp355-363.

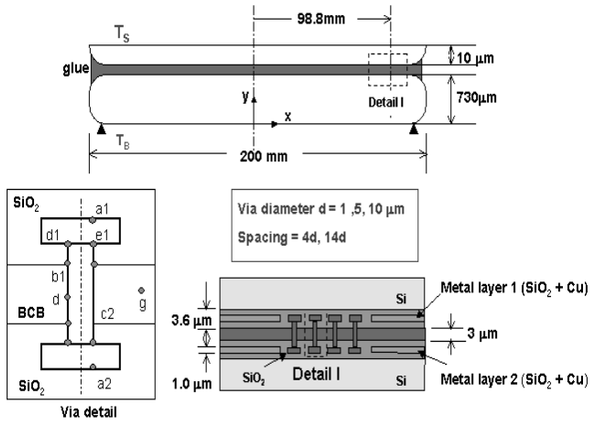

Fig. 1 Schematic of the bonded wafer stack.

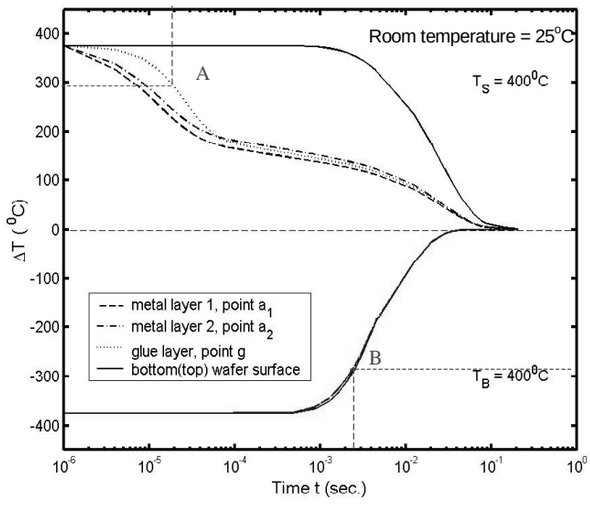

Fig.2 Evolution of transient temperature difference between the interested points and the heated surface.