Study of Plasma Immersion Ion Implantation Induced Damage on Ultra-thin Gate Dielectrics

Ashwin Prasad[1], Vineet Agarwal[2], R.O. Dusane[1] and V.Ramgopal Rao[2]
1. Department of Metallurgical Engineering and Materials Science
2. Department of Electrical Engineering
Indian Institute of Technology, Bombay, Powai, Mumbai-400076, India

Plasma Immersion Ion Implantation (PIII) is a potential process solution for realizing ultra shallow junctions combined with high lateral abruptness. The primary advantage of PIII over conventional beam line implantation is that the implantation time is independent of the wafer size, since the whole target is immersed in the plasma; making the technique ideally suited for 12 inch CMOS processes. However, various process specific issues need to be fully understood, including the plasma implantation induced damage on thin gate oxides, before PIII incorporation into mainstream CMOS device processing becomes a reality.

In this paper, we demonstrate DC PIII to fabricate shallow p^+-n junctions. The DC operation is desirable for extremely high dose rate and monoenergetic PIII applications. We used a parallel plate plasma reactor for the experiments. The implantations were done in the low operating pressure regime (10-25 mtorr) and post implantation annealing was used to activate the dopants. SIMS profiles consistently revealed large peak doping concentrations of the order of 10^{21} cm^{-3}. We have successfully achieved a peak doping concentration of as high as $7x10^{21}cm^{-3}$ with a shallow junction depth. The implanted samples revealed good I-V characteristics with turn on voltages of 0.7 V and low reverse leakage currents.

We also investigate the gate oxide reliability issues posed by PIII, with regards to the charging induced damage. The susceptibility of high-k dielectrics to the induced damage associated with implantation using PIII, is as of now, unknown. We fabricated MOS capacitor structures with antennas, both from SiO_2 and Si_3N_4 dielectrics, for studying the PIII damage. Antenna is a large conducting area connected to the gate of the capacitor, but lying on the field oxide, and serves to accentuate the charging damage. The antenna ratio (the ratio of the antenna area to the gate area) was varied in these devices, and the extent of damage after plasma exposure determined, by a thorough electrical characterization. Implantation parameters were changed in each case so as to establish a correlation between the process parameters and the extent of charging damage.

Substrate (dopant) resistivity	n(P) 0.01-0.03 Ω-cm
Base Pressure	1.5×10^{-5} mbar
Inter Electrode Spacing	5.7 cm
Applied DC Voltage	4 kV

Implantation time	60 sec
Annealing temperature (time=60 sec)	950 ºC
Gas Used	Diborane

Table 1: Implantation parameters for peak doping concentration of $7x10^{21}$ cm^{-3}

Operating Pressure (mtorr)	Peak doping Concentration (cm^{-3})
12	4.66×10^{21}
15	3.066×10^{21}
17	7×10^{21}
22	4.66×10^{21}

Table 2: Operating pressures in DC PIII and the obtained peak doping concentrations

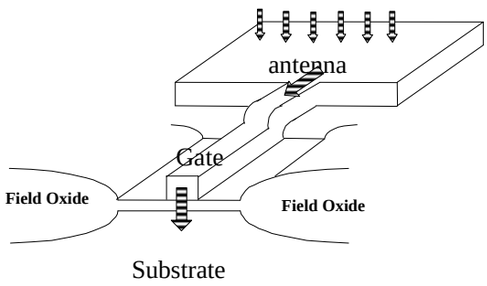

Fig 1: Schematic of an antenna capacitor