Electrical Characterization of Si-SiO_2 and Semiconducting Polymer-SiO_2 Interfaces

M. Jamal Deen

Electrical and Computer Engineering Dept., CRL 226
McMaster University, Hamilton, ON L8S 4K1 Canada
E-mail: jamal@mcmaster.ca

In this paper, we present detailed experimental results from the electrical characterization of silicon-silicon dioxide and semiconducting polymer-silicon dioxide interfaces. For all experiments, we have used field-effect transistors as the device under test (DUT). We have used the following techniques for our electrical characterization studies – current-voltage measurements with the transistor in forward and reverse modes; deep-level transient spectroscopy; and low frequency noise spectroscopy. A main idea of our experiments is to use standard test structures to investigate the semiconductor-oxide interface and not to design and use specialized DUTs. This work reviews and extends our previous work described in refs. [1-7].

With the forward and reverse current-voltage characteristics (role of source and drain interchanged) of MOSFETs, we are able to extract the important parasitic source and drain resistances and to show how the drain resistance evolves as a function of stress-induced damage to the gate-oxide region near the drain junction. These measurements are combined with floating gate measurements to show how the change in drain resistance is correlated with the change in barrier height to electron injection of hot-carriers near the drain junction.

With a new version of deep-level transient spectroscopy (DLTS) – the constant resistance DLTS technique - we are able to accurately investigate interfacial defects in a variety of test structures. With the use of body-bias, we are able to distinguish interfacial and bulk defects that are important for different applications. For example, interfacial defects are important for electronic applications and bulk defects are important for imaging applications. Several examples of results from DLTS studies with and without body bias will be reviewed.

Using low frequency noise spectroscopy and biasing the transistor in saturation, we can spatially profile the defect density near the drain and source terminals for the devices in the normal and reverse modes of operation. Low frequency noise in the linear region also allows us to extract the average defect density over the entire channel region at the silicon-silicon dioxide interface. Recent experiments using bulk bias allows us to look at the contribution of bulk defects – defects away from the silicon-silicon dioxide interface, and its contribution to the device's noise. This is important since substrate biasing is being proposed as a means to cleverly manage power dissipation and speed in emerging circuits and systems.

The second system - semiconducting polymer-silicon dioxide interface – was also studied since polymer devices are being proposed for a variety of niche applications such as electronic tags and drive transistors for displays. For this system, we utilize current-voltage and noise spectroscopy at varying temperatures to study the oxide-polymer interface. Our experiments indicate that the quality of the thin-film transistor depend not only of the type of polymer, deposition conditions and doping, but also on quality of the source electrode-polymer interface near the gate oxide where there could a large concentration of traps. These traps can dominate the carrier transport and can also result in large variations in the devices electrical characteristics, thus making their applications less attractive. Results of current-voltage and low frequency noise measurements from several types of test structures will be presented and discussed.

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