

# Novel Ge Devices with High- $\kappa$ Dielectrics: High Performance MOSFETs and Optical Receivers

Krishna C. Saraswat, Chi On Chui,  
Paul C. McIntyre<sup>1</sup> and Baylor B. Triplett<sup>1</sup>  
Department of Electrical Engineering

<sup>1</sup>Department of Materials Science and Engineering  
Stanford University, Stanford, CA 94305, USA

Historically it has been believed that as the device dimensions are scaled down the high field carrier velocity saturation diminishes the difference in performance of MOSFETs in different materials. However, it has been recently pointed out that a fundamental scaling limit for MOSFETs is the source injection velocity into the channel limiting the drain current [1]. This can be overcome by increasing the low-field carrier mobility. Therefore as the scaling of planar bulk Si CMOS structure reaches its fundamental limits in the sub-20nm regime, innovative device structures and new materials have to be created in order to continue the historic progress in information processing and transmission. Ge is a promising material to overcome the limits of Si due to not only its higher and more symmetric carrier mobility [2] but also smaller mobility bandgap for improved supply voltage scaling and lower contact resistance.

Furthermore its smaller optical bandgap broadens the absorption wavelength spectrum [3] to make attractive for optical interconnects. In particular it may allow heterogeneous integration of optical receivers on Si for clock distribution. Employing optical clocking could eliminate many problems associated with large multi-GHz chips like reducing timing skew, power and area for clock distribution. Performance-wise, a monolithically integrated optical detection system is believed to be better. However, most of the present detection systems use III-V materials in a hybrid integration fashion. Germanium is an attractive material candidate for such a system due to its compatibility with Si and lower fabrication temperature.

Nonetheless, unlike Si, the lack of a stable native oxide hinders the passivation of Ge surfaces [4], resulting in lower mobility, lower drive current and higher leakage in MOSFETs and higher dark current (noise) in optical detection. Common hexagonal GeO<sub>2</sub> phase is thermodynamically unstable and water soluble. During the last four decades, dielectric materials like SiO<sub>2</sub>, SiO<sub>2</sub> on a thin Si cap, Ge<sub>3</sub>N<sub>4</sub>, Ge oxynitride and Al<sub>2</sub>O<sub>3</sub> have been attempted, although none of them would likely offer an EOT of less than 10Å to advance beyond the 20nm regime. Inspired by the recent successes of the high- $\kappa$  deposition technique on Si, we have investigated the possibility of applying high- $\kappa$  to Ge without a native oxide interlayer. Volatility of Ge surface oxides or sub-oxides makes surface cleaning easier for high- $\kappa$  gate dielectric stack free of the performance limiting, lower- $\kappa$ , interfacial GeO<sub>x</sub> layer.

We have demonstrated the use of a high- $\kappa$  gate dielectric material ZrO<sub>2</sub> for passivation of the Ge surface [5]. ZrO<sub>2</sub> was formed using near room temperature UV ozone oxidation [6] of Zr in order to minimize any possible reactions between Ge and the dielectric. MOS capacitors were formed with platinum as the gate electrode. We

achieved excellent  $J_g$ - $V_g$  and C-V characteristics with hysteresis of 1.5mV and a capacitance-based equivalent SiO<sub>2</sub> thickness ( $t_{ox,eq}$ ) of about 6 - 10Å. Additionally, excellent device uniformity and very high device yield were attained. P channel MOSFETs have been fabricated on germanium using a low thermal budget ( $\leq 400^\circ\text{C}$ ) process with high- $\kappa$  gate dielectric and metal gate electrode. For the first time, self-aligned surface-channel Ge *p*-MOSFETs with ZrO<sub>2</sub> gate dielectric with EOT of 6-10 Å and platinum gate electrode are demonstrated in a conventional MOSFET structure with twice the low-field hole mobility than that for Si MOSFETs. A low temperature process to fabricate Metal-Ge-metal (MSM) optical detectors is currently being developed. By combining the MSM optical detectors and the high performance thin film Ge-MOSFETs we are currently investigating integrated optical detection schemes to realize a monolithic optical clocking network.

## Acknowledgements

This work was supported by the DARPA HGI Program, the MARCO Materials Structures and Devices Focus Center, NSF Division of Materials Research, and a Mayfield Fellowship (H. Kim). The authors would like to thank Dr. Ann Marshall, Dr. S. Ramanathan and Dr. C.-M. Park for their invaluable help in processing and characterization.

## References

- [1] M. Lundstrom, *IEEE Electron Device Lett.*, vol. 18, pp. 361-363, Jul. 1997.
- [2] G. E. Stillman, *et al.*, *IEEE Trans. Electron Dev.*, vol. ED-31, pp. 1643-1655, Nov. 1984.
- [3] M. Lee, *et al.*, *APL*, vol. 79, no. 20, p. 3344, 2001
- [4] L. Chang, *et al.*, *Proc. IEEE*, vol. 53, no. 3, p. 316, 1965
- [5] C. O. Chui, *et al.*, *IEEE Electron Device Lett.*, vol. 23, pp. 473-475, Aug. 2002.
- [6] S. Ramanathan, *et al.*, *APL*, vol. 79, no. 16, p. 2621, 2001.