QUANTUM MECHANICAL MODELING OF CAPACITANCE-VOLTAGE AND CURRENT-VOLTAGE BEHAVIOR FOR SiO_2 AND HIGH-K DIELECTRICS

Leonard F. Register, Yang-Yu Fan, Sivakumar P. Mudanai, and Sanjay K. Banerjee

Microelectronics Research Center, The University of Texas at Austin
Austin TX, USA 78758

The scaling of the MOS transistor has effected and will continue to effect many changes in the device. One of the most important of these changes is the expected shift from an SiO_2 gate dielectric to an alternate high dielectric constant (high-K) material. As devices scale so must the, at least, "effective oxide thickness" or "EOT" in order for the gate to maintain control of the channel. However, eventually the direct tunneling current through the scaled SiO_2 becomes unacceptable, depending on application, below around 1.0 to 1.5 nm. The proposed solution is the use of the high-K materials such as Si_3N_4 and HfO_2 that are physically thicker for the same EOT and, thus, are presumably better barriers to tunneling.

However, both the general decrease in EOT and the switch to high-K dielectrics pose many challenges to the continued modeling of gate capacitance and gate leakage currents. Old modeling issues must be reexamined while at the some time new issues are introduced by the change in material system. Among these issues are the capacitive contributions of strong inversion and accumulation layers, the material parameters of the high-K dielectrics, and even the charge transport mechanism or mechanisms through the gate dielectric. High-K materials are typically incorporated into gate stacks including interfacial SiO_2 or silicate layers, complicating the barrier geometry. Perhaps the greatest challenge from a modeling perspective is the absence of knowledge of widely accepted material properties of high-K dielectrics, including band gaps and band-offsets with respect to Si and various metals and complex dispersion relations within the bandgap that are critical for modeling tunneling.

In this work some of the specific requirements and methods for, and some results of accurate modeling of capacitance-voltage (CV) and current-voltage (IV) behavior in ultrathin EOT SiO_2 and high-K gate dielectrics will be discussed [1-4]. It will be demonstrated that, in addition to poly-depletion, rigorous quantum mechanical treatment of accumulation and strong-inversion layers is essential for accurate modeling of capacitance for gate dielectrics with EOTs approaching and below 1 nm, as illustrated by Fig. 1 [3]. It is argued that because of the quantum mechanically enhanced capacitive contribution of the channel strong inversion layer alone, there is an ultimate approximately 0.2 nm limit to the electrical oxide thickness—the thickness that is relevant to the control of the conduction channel by the gate electrode—of MOS devices without even considering the physical thickness of the dielectric layer. It is demonstrated that self-consistent CV and IV calculations are essential for analysis of gate currents, and via such simulation, that the gate leakage current of at least the high-K gate stacks studied are consistent with direct tunneling of carriers through the gate dielectric. It is illustrated how that, even assuming the conduction mechanism is known, calculation of gate leakage currents through high-K gate stacks is complicated by the more complex geometry, the competing effects of variations in dielectric constants, band gaps and offsets and complex bandstructures within the bandgaps. Although the lack of knowledge of these later device properties is problematic as previously mentioned, it is shown that physically accurate and self-consistent modeling of CV and IV, as per Fig. 2, can aid in determining these properties.

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2. S. Mudanai, L. F. Register, A. F. Tasch, and S. K. Banerjee, IEEE Electron Device Letters **22**, 2001, pp. 145-147.
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4. Y.-Y. Fan, R. E. Nieh, G. Lucovsky, G. Brown, L. F. Register, and S. K. Banerjee, IEEE Transaction on Electron Devices, accepted for publication.

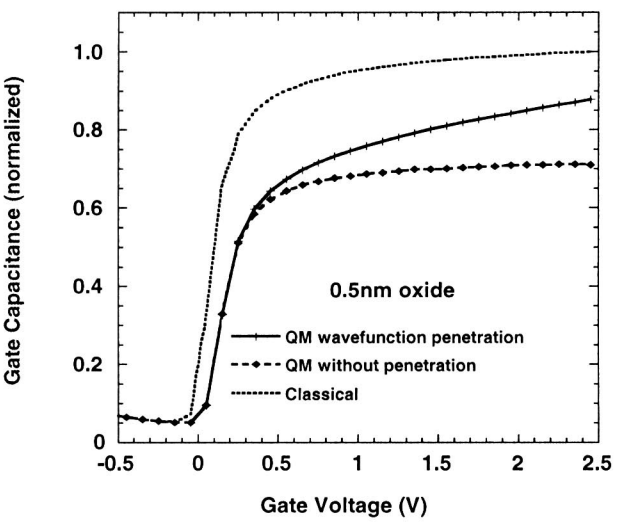
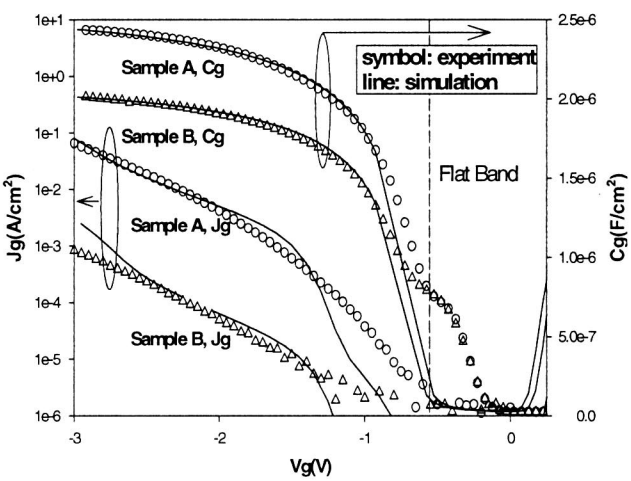


Figure 1. Classical and quantum mechanical calculations of gate capacitance for a 0.5 nm EOT dielectric layer, normalized to the classical value, for a n-channel device in inversion.



Figures 2. Simulation and experimental results for (a) TaN/ZrO_2/Zr-Silicate/p-Si and