What can low-frequency noise learn us about the quality of thin-gate dielectrics?

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Introduction. Low-frequency (LF) noise is generally considered as an undesirable feature in MOSFET technology. Besides unavoidable fundamental noise like shot or thermal noise there exist excess noise sources, e.g., generation-recombination (GR) or flicker noise, which strongly depend on the material and processing quality. This, of course, opens perspectives for using noise as a diagnostic tool. It is largely accepted that one of the main contributors to the excess LF noise is the gate dielectric and more specifically traps in the oxide close to the $Si\text{-}SiO_2$ interface, which have also been called border traps [1].

In this work, a comprehensive overview is given about the use of LF noise for the assessment of the quality of ultra-thin gate dielectrics in deep submicron CMOS technologies. In a first part, the theoretical background of different types of excess noise will be given and what information it can provide us with. In a second part, the impact of the gate dielectric (thermal oxide, NO and RNO oxides) is discussed and illustrated. Evidence will also be presented that LF noise enables the study of gate-related oxide traps. Finally, some future trends will be pointed out.

Theoretical background. One of the basic noise components in small-area devices is a so-called Random Telegraph Signal (RTS) fluctuation [2], which is generated by capture and emission of channel carriers through a single trap center. The corresponding noise spectrum is Lorentzian and enables to study the relevant trap parameters, as a function of gate voltage or temperature. RTSs in the gate current are also a fingerprint for (quasi)breakdown of the gate dielectric (see Ref. 3 and references therein).

It has also been demonstrated that RTS is the fundamental component of flicker noise, which is characterized by a $1/f^{\gamma}$ like spectrum, with $\gamma\sim1$. Based on this so-called number-fluctuations approach, models have been established which enable the extraction of the density of oxide traps N_{ot} from the input-referred noise spectral density [3]. In addition, the study of the frequency exponent γ can yield information on the depth and energy distribution of the oxide traps, if carrier exchange occurs by tunneling [4]. An alternative approach considers thermally activated carrier transitions. In that case, on can derive the energy distribution of the oxide traps from the temperature dependence of γ [5].

Applications. For several reasons, in present-day deep submicron CMOS technologies, thermal oxide is replaced by NO annealed oxides. Besides several advantages, the use of NO oxides gives rise to a strong increase of the 1/f noise, due to the presence of N-related traps close to the interface [3,4,6]. A detailed overview will be given on the impact of nitridation on the noise performance and on measures to improve this.

System-on-a-Chip (SoC) CMOS requires the use of dual gate oxidation techniques. Different approaches are being considered, relying on etch-back [7] or the use of N- or F- ion implantation [3]. As will be shown, this may have a strong effect on the LF noise performance of the devices. Finally, evidence will be provided that gate-related traps in ultra-thin RNO oxides can generate additional excess noise at low frequencies, characterized by a $1/f^{1.7}$ spectrum and this, both in bulk and Silicon-on-Insulator (SOI) transistors.

Conclusions and Outlook. It is clear that the study of LF noise certainly helps to understand the defect physics in thin gate dielectrics. It is expected that in the near future it will also be a useful parameter for characterizing high-k materials and devices and the associated use of metal gates.

References.

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