Process Dependence of Negative Bias Temperature Instability in PMOSFETS

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The threshold voltage shift due to Negative Bias Temperature Instability- NBTI is a major reliability concern, especially for precision analog circuits such as data converters and comparators, which require stable voltage over the lifetime of the circuit.

It has been shown that degradation due to NBTI can be enhanced due to boron penetration, nitrogen content in the film [1,2] and plasma charging [3].

N and P MOSFETs were fabricated on a nominally p-type (100) silicon substrates. The fabrication followed a typical CMOS flow with dual oxide growth. All oxides (2.2nm/6.2nm) were nitrided by a NO anneal step during the last oxidation step. For PMOSFETs gate and source/drain doping was done simultaneously by BF_2^+ (30KeV, 3E15) or $B11^+$ (6KeV, 3E15) implantation. PMOSFETs with L=0.24μm were stressed at 25 °C, 85 °C and 125°C. The gate was held at –4.5V and the well, source and drain were grounded. To study the impact of Nitrogen, thick gate oxide (6.2nm) PMOSFETs were split in 2 categories: with NO anneal and pure thermal oxide without NO anneal.

Fig. 1 shows shift in Vt dependent upon time for different oxides and source/drain and poly implantation. The stress voltage was –4.5V and the temperature 125°C. Transistors with pure thermal oxide and BF_2^+ implant for source drain and gate show minimal amount of Vt shift. This can be attributed to the presence of fluorine, which hinders threshold voltage shifts. Transistors with thermal oxide and B_{11}^+ implant show a higher Vt shift. This is due to the boron penetration. Transistors with NO anneal and with BF_2^+ implant show the highest shift, due to the presence of nitrogen.

Nitridation enhances the generation of positive charges. During stress nitrogen causes an increase in positive charges and interface trap densities. Hence it causes a higher Vt shift [4]. This increase in positive charge and interface traps cannot be compensated by the presence of fluorine.

Fig. 2 shows the lifetime for 30mV Vt shift vs. the inverse of stress temperature (1/T) for different oxides. Thermal oxides and NO annealed oxides have a different slope. The activation energies obtained from the graph show that NO annealed oxides have the lowest activation energy (0.17eV). Thermal oxides show higher activation energy (0.51eV). This is consistent with the observation in [4]. This means that depending upon nitrogen content the maximum allowable operating voltage and temperature will be reduced.

For dual gate processes, nitridation is required to prevent boron penetration. Hence the degree of freedom to modify thick gate oxide processes is limited. However, by carefully choosing the nitrogen content and implant species, the Vt shift can be minimized.

[1] Hook et. al. IBM J. Res. Develop. Vol. 23 No. 3, May 1999.
[2] Chaparala et. al. IRW 2000.
[3] Krishnan et. al. IEDM 2001
[4] N. Kimizuka et. al. VLSI 2000

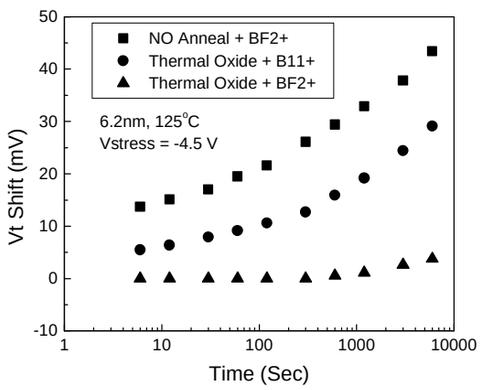

Fig.1 Shift in Threshold Voltage vs. stress time for thermal and NO annealed oxides.

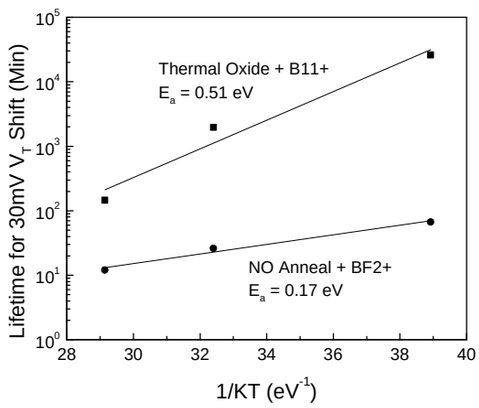

Fig. 2 Activation Energy for thermal and nitrided oxides.