

## **Silicon Dioxide Insulating Films For Silicon-Germanium Technology**

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Silicon-Germanium ( $\text{Si}_x\text{Ge}_{1-x}$ ) insulated-gate metal-oxide semiconductor modulation-doped field effect transistors (MOS-MODFET's) have been investigated to develop CMOS silicon-germanium technology. This paper describes the design, fabrication process and characterization of insulated-gate MODFET devices as a test vehicle to investigate the silicon-germanium technology.

The silicon-germanium heterostructures was grown by molecular-beam epitaxy in a Perkin-Elmer 430S MBE system on a 4-inch 38-63  $\Omega$ -cm B-doped wafer. Except for the supply layer, all epitaxial layers were nominally undoped. However, the background doping of this MBE system is in the high  $1e15/\text{cm}^3$  range, n-type. A 4.5  $\mu\text{m}$  thick graded buffer was first grown, with the germanium concentration increasing from 0 to 30% over this range. A 1  $\mu\text{m}$   $\text{Si}_{0.7}\text{Ge}_{0.3}$  relaxed buffer was grown next. Next, a 5 nm thick layer of  $\text{Si}_{0.7}\text{Ge}_{0.3}$  was grown; this layer was Sb-doped to  $3e18/\text{cm}^3$ . This was followed by an undoped 3 nm thick  $\text{Si}_{0.7}\text{Ge}_{0.3}$  spacer and the 8 nm undoped strained Si channel. A 5 nm thick  $\text{Si}_{0.7}\text{Ge}_{0.3}$  barrier layer and 10 nm thick silicon cap completed the epitaxy.

To fabricate silicon-germanium MOS-MODFET's, the MBE grown structure was cleaned with hot isopropanol, acetone and methanol. No HF dip was performed to protect the thin Si (10 nm) cap layer. Device fabrication was started with a RIE mesa etch to isolate individual devices. The RIE was performed with  $\text{CF}_4$  at 80 sccm,  $\text{O}_2$  at 6 sccm, 100 millitorrs and 50 W for 30 seconds. After the mesa etch, a 5000  $\text{\AA}$  field oxide was deposited by PECVD at 275° C. The parameters for this deposition were  $\text{SiH}_4$  at 15 sccm,  $\text{N}_2\text{O}$  at 33 sccm, RF power 100 W for 16 minutes. Measured oxide thickness was 5100  $\text{\AA}$ . Windows were then etched in the field oxide with buffered HF (BHF) to define the source and drain regions. The source and drain were formed by ion-implantation with phosphorus at 25 KeV at a dose of  $3e15/\text{cm}^2$ , with a tilt angle of 7 degrees. The gate region was then opened by etching with BHF.

The gate oxide was grown in a two step process. Thermal oxidation was carried out at reduced temperature (750° C) to produce a thin, high quality gate oxide. PECVD disposition was then used to thicken the oxide to 1200  $\text{\AA}$ . First, a lithography step was used to remove the field oxide from over the gate region. The standard lithography procedure was used, followed by immersion of BHF to remove the oxide.

After the hard-bake the wafer piece was immersed in buffered HF (BHF) for about 4 minutes with gentle agitation to remove the oxide from the gate area. Electrical probing was used to verify complete removal. The wafer was rinsed and dried.

The oxidation furnace was set to a temperature of 750° C and the oxygen flow rate set to 500 sccm. The oxygen was bubbled through trichloroethylene (TCE) to help improve the quality of the gate oxide. The wafer was oxidized for 45 minutes in dry oxygen to yield an oxide thickness of 30  $\text{\AA}$ . The oxygen was then bubbled through water containing a few drops of hydrochloric acid at 95° C.

Oxidation in this wet ambient was allowed to continue for 45 minutes, yielding a oxide thickness of 170  $\text{\AA}$ , after which the bubblers were switched back to dry oxygen/TCE for another one hour to yield an additional oxide of thickness 30  $\text{\AA}$ . The oxygen was then replaced with dry ultra-high purity (UHP) nitrogen and the wafer was then annealed in this nitrogen ambient for 10 minutes before being removed from the furnace. The temperature was maintained at 750° C throughout. The oxide thickness was measured with the ellipsometer and found to be 230  $\text{\AA}$ . The wafer was then loaded into the reaction chamber of the Technics PEIIA/PDIIA plasma system for PERCVD oxide deposition. Deposition was carried out at a platen temperature of 275° C for 190 s using  $\text{SiH}_4$  of 15 sccm,  $\text{N}_2\text{O}$  of 33 sccm at 275° C.

Ellipsometric measurement indicated a total oxide thickness of 1200  $\text{\AA}$ . The wafer was then subjected to a rapid thermal anneal (RTA) in a pure hydrogen ambient to reduce the density of dangling bonds at the Si-SiO<sub>2</sub> interface, and hence improve oxide quality. Then hydrogen was introduced at 1.5 slpm, the temperature increased to 350° C, held for 30 minutes and cooled to room temperature in a nitrogen ambient. A lift-off process was used for source and gate contacts. 500  $\text{\AA}$  of Al/2%Si were deposited, followed by 3500  $\text{\AA}$  of Au, without breaking vacuum.

The current-voltage characteristics as well as transfer characteristics of the devices at room temperature demonstrated the feasibility of using n-channel and p-channel MODFET's for power devices as well as for digital circuits.