ELECTRICAL CHARACTERIZATION OF THIN OXIDE LAYERS BY IMPEDANCE SPECTROSCOPY USING SILICON/OXIDE/ELECTROLYTE (SOE) STRUCTURES.

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As a consequence of technology scaling, advanced gate dielectric coatings, a few atomic layers in thickness, are required in the new chip generation. Capacitance/voltage (C/V) characteristics is a fundamental property of the MOS devices. A precise measurement of the device capacitance is a determining step for the oxide thickness setting and channel length determination. It is recognized that capacitance measurements become difficult because of the high tunneling leakage current.

For this reason we studied[1] the electrical characteristics of surface silicon oxides by electrochemical impedance spectroscopy (EIS). In this method the measurements are performed, at zero current for various bias voltage values, using a SOE structure semiconductor/oxide/electrolyte. In this case, the solvated ions in solution are not subject to tunneling phenomena.

The study was mainly carried out using thermally oxidized p-Si wafers, 100 oriented, 200 mm diameter. Three sample series were studied, the oxide thickness being 1.2, 2.4, and 4.5 nm respectively. The electrolyte was a deaerated 0.1 M HCl solution.

From our measurements of impedance diagrams, we obtained the appearance of nice semi-circles, thus indicating that the interface can be modelled as parallel RC loops. Moreover, at negative bias potential and in the dark, we observed a second RC loop which was identified as corresponding to the p-Si depletion layer since the capacitance value was a few 10^{-2} µF/cm^2, whereas the capacitance of the oxide layer was in the range of a few µF/cm^2. The equivalent circuits were modelled as loops involving a constant phase element (CPE). The quantitative data treatment, using the Boukamp software, proved that the imaginary component was a pure capacitor C in parallel with a purely ohmic resistance R.

Fig. 1 shows a few examples of EIS Nyquist diagrams obtained, in the dark, for bias potentials values from +1.0 to –1.0 V *vs* SCE reference electrode. Curve a obtained at +0.2 V and for more positive bias potentials, only shows an almost vertical line due to the purely capacitive behaviour of the oxide layer; indeed, the parallel resistance of the highly insulating thermal oxide layer was found equal to several 10^8 Ω.cm^2 for a 22 Å thickness. Curves d, e, and f were obtained with the same sample polarized at –0.4, -0.6, -0.8 V/SCE, showing the appearance of another RC loop revealing the formation of a highly resistive depletion layer within the substrate.

An interesting feature of our method is that the overall measured impedance can be separated into two components one corresponding to the depletion layer and the second to the oxide film. Nevertheless, the capacitance/voltage characteristics of the oxide insulator alone was found to fit the analytical expressions of the mobile charge distribution within the semiconductor. Indeed the charge of the oxide layer capacitor is limited by the charge process of the semiconductor interface.

Starting from the flat band potential, the charge Q accumulated in the semiconductor space charge as a function of the surface potential Φ_S is given by:

$$Q = 2\varepsilon\varepsilon_0[N_A e\,\Phi_S + N_A kT(e^{-e\,\Phi_S/kT} - 1) + n_0 kT(e^{e\Phi_S/kT} - 1)]^{1/2}$$

Where $n_0 = n_i^2/N_A$ represents the generation of minority carriers which contribute to the inversion layer formation. Moreover our study leads to the determination of the resistance term in the space charge region. Fig.2 shows the variation of the oxide capacitance versus the overall applied potential. The slope of the capacitance variation is much less in the accumulation zone than in the inversion zone, as it could be predicted from the gradient of electrical potential derived from the resistance term.

Further on, fig.2 exhibits the strong influence of light, with the generation of hole and electron pairs, on the depletion branch whereas the effect was negligible on the accumulation branch thus supporting the interpretation based on the local electric field.

Results obtained with this careful method lead to the oxide capacitance values in excellent agreement with the predicted values from the oxide thickness obtained by ellipsometry.

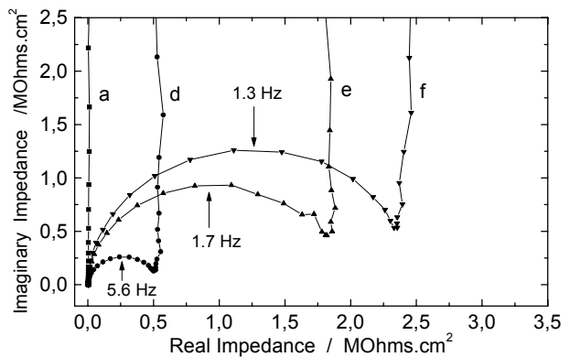

Fig.1 : Impedance diagram, in the dark, of p-Si coated with 22 Å oxide at applied bias potential values: a +0.2, d –0.4, e –0.6, f –0.8 V *vs* SCE.

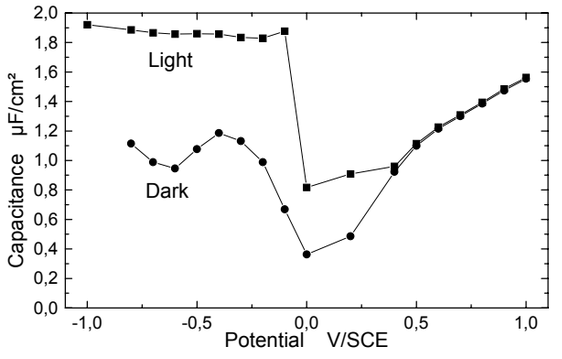

Fig.2 Capacitance *vs* potential of a 22 Å thermal oxide layer.

References:

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2- M. Chemla, V. Bertagna, R. Erre, F. Rouelle, S. Petitdidier, D. Lévy, *Electrocheical and. Solid State Letters.* **6**, G7 (2003)