Decoupled Plasma Nitridation of Ultra-Thin Gate Oxides for 65 - 90nm technologies.

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Introduction

It is of common knowledge that the continuous scaling of gate oxides down to 1.6nm and below will soon require the integration of high-κ dielectrics as Al_2O_3 or HfO_2. However, even the most promising candidates still face a number of stopping issues as micro-crystallization upon heating or fixed charges [1-2]. Therefore, we've rather developed alternative medium-κ silica-based oxides using a decoupled plasma nitridation technique (DPN). This process allows incorporating a large dose of nitrogen at the silica top surface leading to thinner equivalent oxide thickness (EOT), reduced gate leakage and lower negative bias temperature instability (NBTI) degradation (not reviewed in the present abstract).

Experimental

CMOS transistors with a nominal gate length of 70nm were fabricated, table 1. Wafers were first oxidized in a single wafer equipment to grow 1.4-1.6nm pure RTO pre-oxides. Subsequently, oxidized samples were nitrided in a separate DPN chamber. An additional high temperature oxidizing anneal was required to stabilize the nitrogen incorporation. Next, 150nm polysilicon was deposited. Rapid thermal nitrided (RTN) oxy-nitridation was considered as our reference process (950°C, 30s, NO).

Results and Discussion

EOT and flat band voltages (V_{FB}) were computed after simulating C-V measurements with the CVC simulation software, figure 1, [3]. EOT were found to decrease down to 1.4nm for an optical thickness of 2.2nm, owing to an increase of the material permittivity. V_{FB} were driven by both the N dose and the location of N atoms in the silica bulk: In case of light DPN conditions, N species were piling up at the oxide top surface (DPN-2, low V_{FB}) whereas they were extending in the SiO_2 bulk for hard DPN conditions (DPN-1, V_{FB} similar to RTN), figure 2. Next, gains in gate leakage up to 5x (10x) were computed with respect to RTN (pure RTO) films, figure 3. An excellent within wafer uniformity of the gate leakage, i.e. of the EOT, was reported.

Present Limitations

First, a deleterious physical reoxidation of the material was assumed when decreasing the bottom oxide thickness preventing from a continuous scaling of the EOT, figure 4, [4]. Second, the extension of the N profile to the Si-SiO_2 interface for high N dose was supposed to degrade the channel mobility, then the performances. Finally, a clear within wafer non-uniformity of the N incorporation was outlined using different in-line techniques, such as delay-to-reoxidation measurement (detailed in the paper), leading to a large range of threshold voltage values.

References

1. A.L. Rotondaro et al., *Symp of VLSI Tech*, p.148 (2002)
2. K. Torii et al., *Symp of VLSI Tech*, p.188 (2002)
3. J.R Hauser, *Charac Metro for ULSI Tech*, p.235 (1998)
4. C. Chen et al, *IEEE Trans Elec Dev*, **49** (5), 840 (2002)

ID	Gas	P (Torr)	RF (W)	Time (s)
DPN-1	N_2, He	20.10^{-3}	500	35
DPN-2	N_2	5.10^{-3}	300	10

Table 1 – DPN process conditions

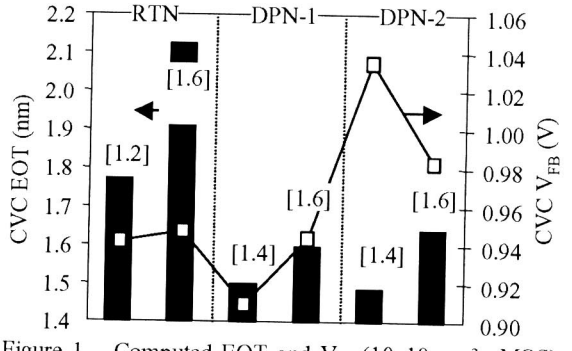

Figure 1 – Computed EOT and V_{FB} (10x10 µm² pMOS) Optical pre-oxide thickness are given in brackets (in nm)

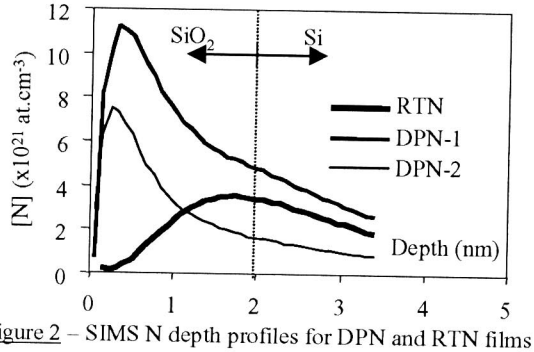

Figure 2 – SIMS N depth profiles for DPN and RTN films

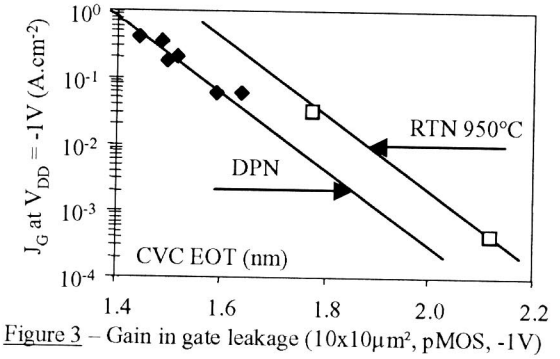

Figure 3 – Gain in gate leakage (10x10µm², pMOS, -1V)

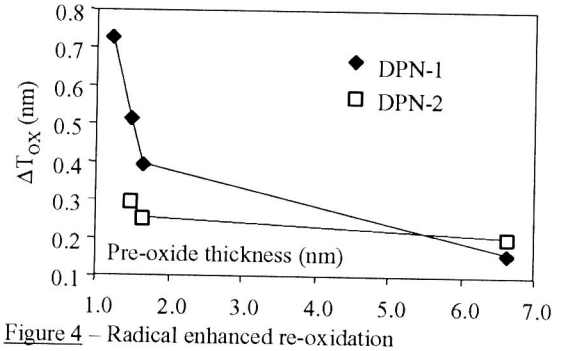

Figure 4 – Radical enhanced re-oxidation