Plasma nitridation optimization for sub-15Å gate dielectrics

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Sub-100 nm CMOS technologies require gate dielectrics below 1.5 nm equivalent oxide thickness (EOT). The introduction of nitrogen (N) in the gate oxide using furnace nitridation has been shown to minimize B penetration and reduce the gate leakage current. However for sub-15 Å gate dielectric, aggressive nitridation processes such as plasma nitridation techniques are required to extend SiO_2 based gate insulator technology. In this work, ultra-thin plasma nitrided dielectrics down to 12 Å have been produced by a decoupled plasma nitridation (DPN) process. The impact of process parameters upon physical properties and upon the electrical performance has been studied.

The gate dielectrics were formed in three steps:1 - Growth of a pure thin oxide film using in-situ steam generation oxidation (ISSG). Various thicknesses were grown. 2 - Nitridation using a DPN process. In this work, the plasma nitridation time and percentage of helium (He) in the reaction chamber were studied. 3 - Post Nitridation Anneal (PNA). The effect of a PNA as well as the temperature and time of this anneal were investigated. The chemical structures of oxynitride films were studied by x-ray photoelectron spectroscopy (XPS) and by angle-resolved XPS (AR-XPS). Sub-100 nm n- and p-MOS transistors were fabricated to evaluate the sub-15 Å oxynitrides. Capacitance-Voltage (C-V) characteristics of MOS capacitors with gate oxynitrides down to 12 Å have been accurately measured at RF frequencies (~GHz) as illustrated in figure 1. EOTs and flat-band voltages (V_{FB}) values were extracted from CV measurements.

An example of XPS spectra of N 1s for different plasma nitridation times is shown in figure 2. It can first be observed that only one N 1s peak position was measured at a binding energy of 397.7 ± 0.1 eV. This binding energy is close to the reported binding energy for the Si-N bond in Si_3N_4. When increasing the nitridation time, the intensity of the N 1s peak increases corresponding to an increase of N in the silicon-(oxi)-nitride film. The consequence of this increase of N in the oxynitride film is also observed in the electrical characteristics shown in figures 3 and 4. Larger N incorporation results in a lower gate leakage current density (J_G), as illustrated in figure 3. This is consistent with previous results regarding N increasing the dielectric constant (ε) of the film; an increase of N also leads to a physically thicker film reducing the gate leakage current. A slight decrease in EOT with increasing the N content is seen for the thickest base oxides. This EOT reduction is not observed for the thinnest base oxides. This will be discussed further in the final paper. There is therefore a trade-off between the amount of N in the oxide, the reduction in $J_{G,}$ and the scaling of the dielectric. Moreover, when increasing the plasma nitridation time, a shift of V_{FB}, an increase of the linear subthreshold slope, and a degradation of the maximum of the normalized transconductance (used as an indicator of the carrier mobility) are observed (Fig. 4). This could be attributed to the creation of fixed charges in the bulk with the incorporation of N, and/or to the creation of interface states. The amount and location of the N atoms is therefore of primary importance in the gate dielectric optimization and will be discussed further in the final paper.

This work focuses on the understanding of the various parameters of the plasma nitridation process used to form ultra-thin oxynitrides. It is shown that an effective compromise between EOT-J_G reduction and mobility degradation can be obtained with the appropriate plasma nitridation and anneal conditions.

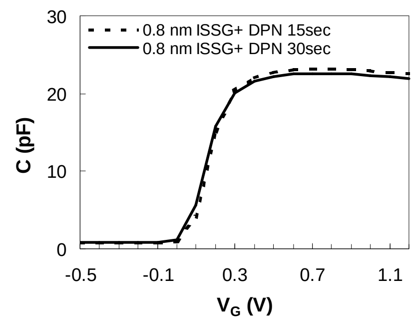

Figure 1: RF-C-Vs of ultra-thin gate oxynitrides measured at 0.534 GHz. 1.2 and 1.3 nm EOTs were calculated for oxynitride with a plasma nitridation of 15 and 30 sec respectively.

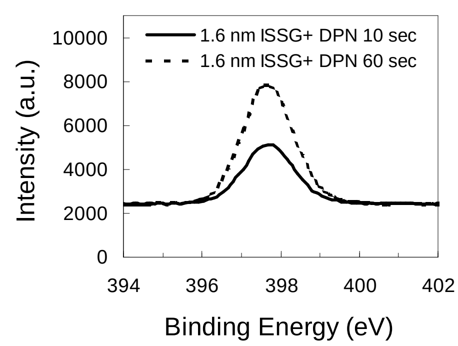

Figure 2: Core level spectra of the N 1s obtained at an angle of 45°.

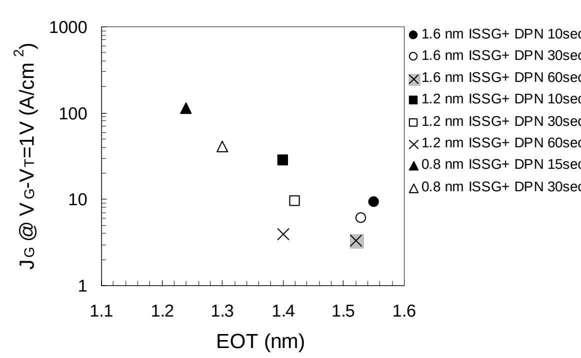

Figure 3: Gate leakage current density measured on NMOS transistors as a function of EOTs.

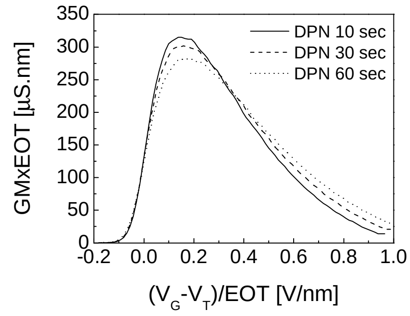

Figure 4: Normalized transconductance of NMOS transistors having a 1 µm gate length.