## SC1 Cleaning Effect on Electrical Characteristics of 256M-bit mobile DRAM with Dual Gate Oxide

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In the sub-0.15μm design rule, a 256M-bit mobile DRAM operating at $V_{DD}$ = 1.8 V requires a new fabrication process, which has a thin gate oxide in the logic area for high speed, a thick gate oxide in the high $V_{DD}$ (≥3.5V) region for a higher reliability (1). Therefore, the electrical characteristics and microstructures were investigated with SC1 cleaning time split (0, 150, 300, 600 seconds) before the second gate oxidation. After forming the STI definition and adjusting channel, the gate oxide of pure dry $SiO_2$ was grown at 850℃ with a physical thickness of 6.5 nm, and then the region of the thin (5.0 nm) and thick (7.8 nm) gate oxides was separated by added resist patterning. After removing the first gate oxide in the thin oxide region by the buffered oxide etchant and the second gate oxide was grown to a physical thickness of 5.0 nm of pure dry $SiO_2$ at 850℃. After patterning gate, conventional CMOS processes were done. The thick gate oxide thickness was highly decreased compared to the thin gate oxide with increasing SC1 ($NH_4OH$: $H_2O_2$: $H_2O$ = 1:4:20, 70°C) time (Fig.1). The etching rate of the thick oxide by SC1 cleaning was approximately 1.60 Å/min. In our case, the cleaning condition before the second gate oxidation was only SC1 cleaning without a subsequent HF clean, which caused an oxide defect failure in the thick oxide region. SC1 cleaning affects the etching rate for Si substrates surface and $SiO_2$ with concentration and cleaning time (2). In the thick oxide MOSFETs, the Vthn increased and the |Vthp| decreased due to no photolithography steps for adjust the Vth of the thick oxide MOSFETs (Fig. 2 and Fig. 3). It is important that the decrease of gate oxide thickness and the boron concentration affected by SC1 cleaning has an influence on the Vth because boron doses are segregated into the Si substrates surface and $SiO_2$ layer. Especially, this segregation is getting more in the dual gate oxide process due to increased gate oxidation time. In the thin oxide MOSFETs, Vthn seems to be not different, however, |Vthp| increased with increasing SC1 time. In the thick oxide MOSFETs, Vthn decreased, however, |Vthp| increased with increasing SC1 time. Consequently, NMOSFETs were found to be more dependent on the decrease in the gate oxide thickness than boron doses, however, PMOSFETs seemed to be more dependent on the decrease in the boron doses than the gate oxide thickness due to the different channel boron depths, which were 1000Å for NMOSFETs and 450Å for pMOSFETs by SIMS (not shown here). The RMS roughness with SC1 time remarkably increased for SC1 600 seconds (Table 1). It means that the etching structures of Si substrates surface and $SiO_2$ oxide depend on SC1 time. Therefore, the SC1 cleaning condition is considered to be controlled under 300 seconds considering the Vth fluctuations and RMS roughness of samples.

1. Hoon Lim *et al*, 39th Inter.Rel.Phy.Sym, p.48, 2001
2. K. Yamamoto et al., IEEE trans., vol.12, p.288, 1999

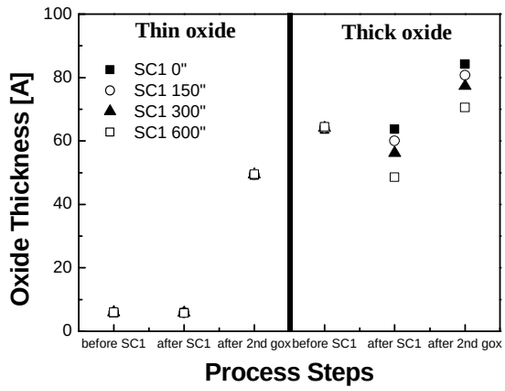


Fig. 1 The distribution of the gate oxide thickness measured by ellipsometer as steps.

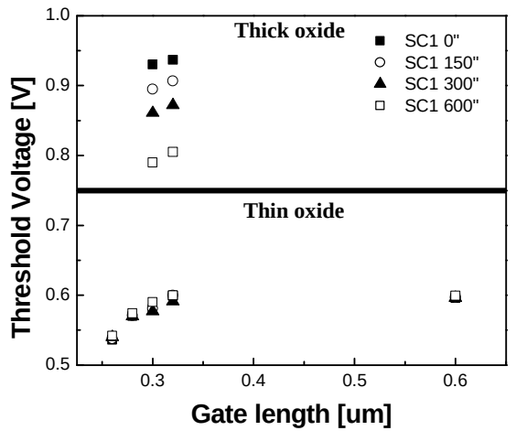


Fig. 2. The threshold voltages (Vthn) of nMOSFETs as a function of the gate length.

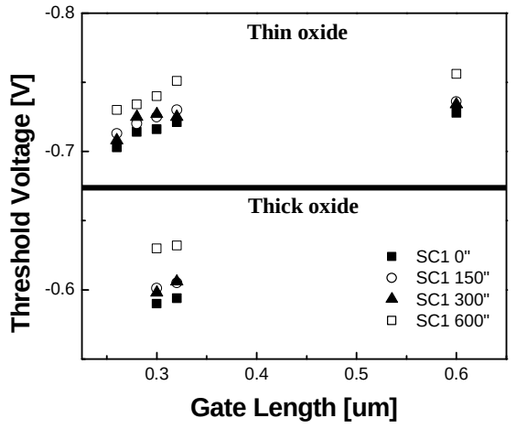


Fig. 3. The threshold voltages (Vthp) of pMOSFETs as a function of the gate length.

Table 1. AFM data (RMS roughness) of Si substrates surface and the gate oxide surface after SC1 cleaning.

| Step | Thin Tox | Thin Gox RMS | Thick Tox | Thick Gox RMS |
|---|---|---|---|---|
| SC1 0" | 0.584nm | 0.215nm | 6.369nm | 0.226nm |
| SC1 150" | 0.586nm | 0.223nm | 6.409nm | 0.233nm |
| SC1 300" | 0.587nm | 0.221nm | 6.406nm | 0.239nm |
| SC1 600" | 0.590nm | 0.274nm | 6.444nm | 0.259nm |