Effect of Post Oxidation Annealing on VCSEL Device Performance

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The vertical cavity surface emitting laser (VCSEL) devices has many important applications as optoelectronic device including low power and high frequency light source, multiwavelength hyperspectral imaging, surveillance and target acquisition, sensor fusion and signal intelligence. Generally ion-implantation or wet oxidation process is used for VCSEL devices fabrication for current confinement in mesa structure [1]. Most of the reported reports on wet oxidation process for aperture control deal with the various oxidation times and its relation to threshold current for laser emission. However, it is well known that wet oxidation technique creates trapped oxide charge and interface traps in the oxide [2]. We report here the results of our experiment on annealing of VCSEL devices after oxidation at different temperatures and times. As it is seen in Fig. 1, significant improvement (about 18% increase) in out put emission power of the VCSEL is observed by annealing in nitrogen environment at 400 C. Unlike previous reports [2], in which the authors reported reduction in voltage drop after high temperature annealing, we observed an increase in voltage drop of the device.

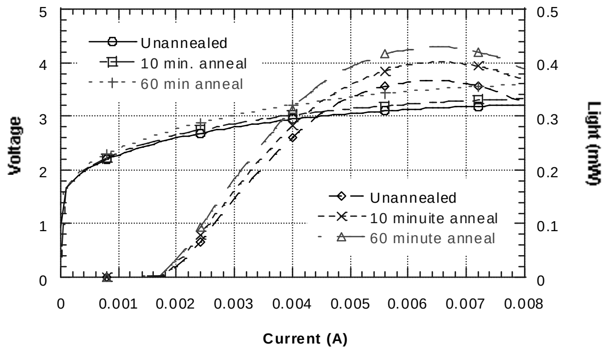

Figure 1. I-L-V characteristics with and without anneal

We used 850 nm top emitting VCSEL structure with 25 pairs of top p-mirror and 35 pairs of bottom n-mirror. The active region contains three 7.0 nm wide GaAs quantum wells separated by 7.0 nm wide $Al_xGa_{1-x}As$ barriers. The detail of VCSEL fabrication is reported in a separate publication [3]. The top 1000 Ang. GaAs contact layer is doped with beryllium to a concentration of $3x10^{18}$ /cm^3 to achieve a good ohmic contact. Wet oxidation was carried out at the temperature of 400 °C with nitrogen carrier gas bubbled through H_2O at 85 °C for current confinement. Ti/Au (300/2500 Å) metal film was deposited as a p-type contact metal on the topside and Ge/Au metal film was deposited as an n-type metal on the backside of the wafer. Annealing was carried out in nitrogen environment after complete fabrication of the device. The annealing temperature was varied between 380 to 425 C. To determine the reason for enhanced light output, we measured the Capacitance and Voltage (C-V) curve of a test mesa structure before and after annealing. The test structure for capacitance measurement is on the same wafer as VCSEL device. The high frequency (1 MHz) capacitance-voltage curve was taken by using a HP 4280A model C-V meter. After annealing in nitrogen environment, the C-V curve shifts (Fig. 2) to more negative gate voltages indicating reduction in negatively charged traps. We also observed a little change in slope of the C-V curve of annealed device compared to unannealed device, which indicates reduction in interface traps. Hence it is concluded that the observed increase in VCSEL light out put after annealing is due to reduction in negatively charged traps and interface states at GaAs and oxide interface in mesa structure.

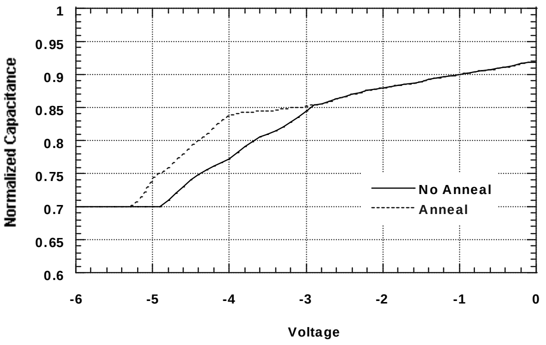

Figure 2. C-V characteristics with and without anneal

Acknowledgements: We thank P.Shen and P. Newman for their help in the experiments.

[1] D.L. Huffaker and D.G. Deppe, Appl. Phys. Lett, 70, 1782 (1997)
[2] K.Y. Lim, J.Y. Kim, Y. Hayashi, T. Mukaihara, N. Ohnoki, F. Koyama and K. Iga, J. of Korean Physical Society, V.28, 495 (1995)
[3] N.C. Das, B. Gollsneider, P. Newman and W. Chang, Appl. Physics Letters, V. 81, 1600 (2002)
[4] W.T. Tsang, Appl. Phys. Lett, 33, 426 (1978)