## A study on selective $Si_{0.8}Ge_{0.2}$ etch using polysilicon etchant diluted by $H_2O$ for three-dimensional Si structure application

Sung-min Kim, Chang-woo Oh, Jeong-dong Choe, Chang-sub Lee, and Donggun Park

Advanced Technology Development Team, Device Solution Network Samsung Electronics Co. Ltd Giheung-Eup San 24, Youngin-City, Kyunggi-Do Korea 449-711 E-mail: <u>sanaii.kim@samsung.com</u> Tel:82-31-209-6679 Fax.:82-31-209-3274

## Abstract

To overcome the difficulties of transistor scaling, three-dimensional structures like silicon on nothing (SON) or gate all around (GAA) structure using SiGe have been investigated<sup>1-2</sup>. For the implementation of these structures, c-SiGe etch techniques with high selectivity to c-Si are required. As one of the approaches, we performed the wet-etch experiments using polysilicon etchant for the samples with epitaxially grown c-Si and c-SiGe layers on silicon substrate.

In Si<sub>0.8</sub>Ge<sub>0.2</sub> wet etch, we diluted polysilicon etchant, which is composed of 40:1:2:57, HNO<sub>3</sub> (70%):HF (49%):CH<sub>3</sub>COOH (99.9%):H<sub>2</sub>O, with H<sub>2</sub>O to control etch rate and selectivity. Figs. 1 and 2 show the etch rate and the selectivity depending on diluent H<sub>2</sub>O volume, varied from 0 to 5 volumes, with the polysilicon etchant held constant at 10 volumes, respectively. Figs. 3 (a) and (b) show the scanning electron microscope (SEM) images for the samples etched in low and high H<sub>2</sub>O volumes. As shown in the figures, as the H<sub>2</sub>O volume was increased, the excellent etch condition with low etch rate and high selectivity was obtained. It was thought that H<sub>2</sub>O didn't affect the increase of selectivity directly and that the decrease of HNO3 volume due to H2O dilution mainly caused those effects as pointed by the previous researchers<sup>3</sup>

Conclusively, using the optimized condition, we could successfully etch single crystalline  $Si_{0.8}Ge_{0.2}$  layers with the selectivity higher than 300:1 and easily obtain a SON structure as shown in Fig. 4. The newly developed etch condition for  $Si_{0.8}Ge_{0.2}$  are very useful to the fabrication of three-dimensional FET or the similar structure to silicon on insulator (SOI).

## **References**

<sup>1</sup>S. Monfray, *et al.*, *Tech. Dig. of IEDM 2001*, pp. 645-648, 2001.

- <sup>2</sup>S. Monfray, et al., Tech. Dig. of Symp. on VLSI Tech. pp.108-109, 2002.
- <sup>3</sup>G. K. Chang, T. K. Carns, S. S. Rhee, and K. L. Wang,
- *J. Electrochem. Soc.*, Vol. 138, No. 1, pp. 202-204, 1991. <sup>4</sup>D. J. Godbey, A. H. Krist, K. D. Hobart, and M. E. Twigg, *J. Electrochem. Soc.*, Vol. 139, No. 10, pp. 2943-2947,
- <sup>5</sup>K. Koyama, M. Hiroi, T. Tatsumi, and H. Hirayama,
- K. Koyama, M. Hiroi, T. Tatsumi, and H. Hirayama, *Appl. Phys. Lett*, Vol. 57, No. 21, pp. 2202-2204, 1990.



Fig. 1. The changes of etch rate depending on  $\mathrm{H}_2\mathrm{O}$  volume.









Fig. 3. The cross sectional views of (a) the sample etched with the polysilicon etchant (b) the sample etched with the newly developed  $Si_{0.8}Ge_{0.2}$  etchant with high selectivity.



Fig. 4. The SON structure fabricated by using the newly developed  $Si_{0.8}Ge_{0.2}$  etchant with high selectivity.