Relaxed SiGe-On-Insulator substrates through implanting oxygen into pseudomorphic SiGe/Si heterostructure

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SiGe-on-insulator (SGOI) attracts great interest due to its potential for realizing strained Si with in-plane tensile strain, which results in enhanced carriers mobility. SIMOX, ion-cut (or commercially Smart-cut) and BESOI, have been explored to form SGOI novel structures. However, they are yet far from massive industrial applications. Two main reasons are cost and performance. Both SiGe film growth and SIMOX/Ion-cut/BESOI process require strict technologies and thus are costly. Therefore simplifying the fabricating processes for SGOI structures to lower the cost is quite necessary. On the other hand, SGOI performance should be further improved.

Among the three fabrication methods, SIMOX is competing for SGOI fabrication. Nevertheless, most of previous studies use SiGe materials with a thick SiGe buffer and result in SiGe/SiO2/SiGe/Si structures. This thick buffer is important in suppressing Ge loss during high temperature annealing [1]. However, besides high cost, the buffer causes some problems. Using the buffer layer, the implanted oxygen locates in the SiGe layer, Ge has to be rejected from the oxygen-rich region to form SiO2 buried layer. For a high Ge composition, this is even not feasible at all. So there is an upper Ge limit (about 14%[1]) for SiGe SIMOX. Most of previous work successfully resulting in SGOI adopted SiGe with a Ge concentration of 10% as the SIMOX target. Meanwhile, the thick buffer brings a dilemma on choosing the annealing temperature. The decreasing melting point of SiGe with increasing Ge concentration allows lowering annealing temperature, whereas the formation of buried silicon dioxide layer requires higher temperature.

In this study, we developed a modified SIMOX process for fabricating SGOI substrates without using thick SiGe buffer structures. A 115nm thick SiGe film with uniform Ge composition of 16% is pseudomorphically grown on Si (100) substrate without any buffer layer. An additional 8nm Si cap layer is grown to prevent SiGe from possible sputtering during ion implantation. Then 3x1017cm-2 of O+ is implanted into the interface of SiGe/Si substrate at 550oC. A two-step annealing is used to suppress Ge loss. This may contribute to overcoming the Ge upper limit for SiGe SIMOX and is more fit for ultra-thin relaxed SGOI fabrication. The first step at a modest temperature is to improve the block ability of buried layer to Ge diffusion, and the second step with a high temperature is to form the buried silicon dioxide layer with high quality. Rutherford backscattering spectroscopy (RBS) is used to monitor Ge loss, rocking curve is employed to characterize the recovery of implantation damage and also the strain in SiGe. We have experimentally demonstrated SGOI structures with reduced Ge loss, and high relaxation rate.

1. N.Sugiyama, T.Mizuno, M.Suzuki, and S.takagi, Jpn,J.Appl.Phys., Part1 40, 2875 (2001).

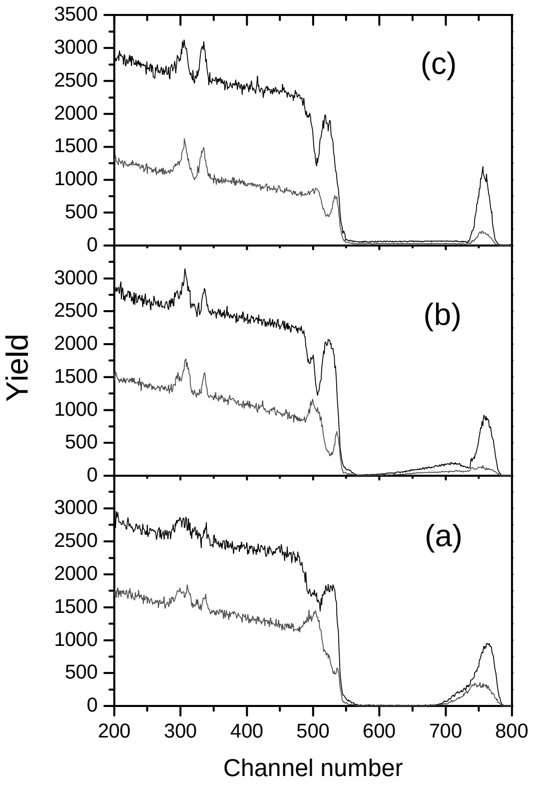

Fig.1 RBS/C of samples with different annealing process. (a: annealed at 1150^{o}C for 30 minutes; b: annealed at 1000^{o}C for 3 hours; c: annealed at 1300^{o}C for 4 hours).

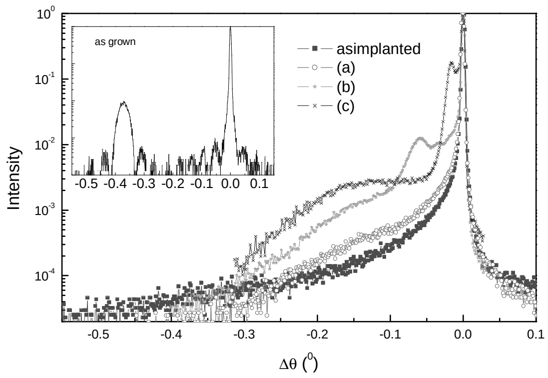

Fig.2 Rocking curves of samples with different annealing process.

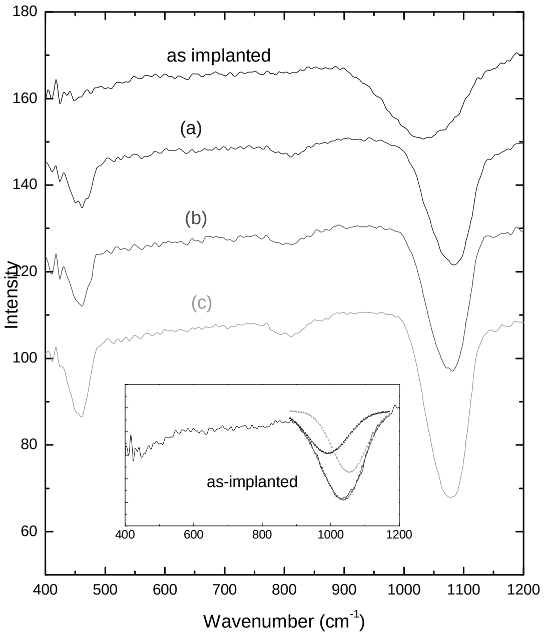

Fig.3 Fourier transform infrared spctroscopy of samples with different annealing process.