

## Replacing the BOX with Buried Alumina: Improved Thermal Dissipation in SOI MOSFETs

K. Oshima<sup>1,4</sup>, S. Cristoloveanu<sup>2</sup>, B. Guillaumot<sup>3</sup>,  
G. Le Carval<sup>1</sup>, H. Iwai<sup>4</sup>, C. Mazuré<sup>5</sup>, M.S. Kang<sup>6</sup>,  
Y.H. Bae<sup>7</sup>, J.W. Kwon<sup>8</sup>, J.H. Lee<sup>8</sup>, S. Deleonibus<sup>1</sup>

- (1) CEA LETI/DTS/SRD, 38054 Grenoble, France
- (2) IMEP, ENSERG, 38016 Grenoble, France
- (3) STMicroelectronics, Central R/D, Grenoble, France
- (4) Tokyo Institute of Tech., Yokohama, Japan
- (5) SOITEC, 38190 Bernin, France
- (6) COMTECS, Daegu, Korea
- (7) Uiduk Univ., Kyongju, Korea
- (8) Kyungpook National Univ, Daegu, Korea

In this paper, we propose a conceptual modification of the SOI structure, by replacing the buried oxide with an alternative dielectric. Such generalized-SOI structures open new fields of application and improve the performance of CMOS devices. We focus on the critical problem of self-heating which is responsible for degradation in mobility, threshold voltage, sub-threshold swing, leakage current, etc.

Since self-heating is mainly due to the poor thermal conductivity of the buried oxide (BOX), an elegant solution is to replace the BOX with buried alumina (or other dielectric), which offers much higher thermal conductivity (by more than one order of magnitude). The resulting material is still SOI-like — thin Si-film, high-K dielectric, Si substrate — and can be synthesized by adapting the current bonding techniques. SOI-like structures with buried alumina have been manufactured: the process flow will be described and preliminary characterization results will be reported.

2-D simulations of transistor temperature have been performed with SILVACO tools. It is clearly observed that the temperature in the channel of advanced SOI MOSFETs is substantially lowered by replacing the BOX with buried alumina. Extensive simulations will be discussed. However, in order to emphasize the critical role of the buried insulator, an analytical model is proposed, based on the simple structure of the SOI device.

The total thermal resistance of the transistor is calculated by accounting for the heat flow through gate, source, drain and substrate. An equivalent thermal circuit is conceived, which includes detailed contributions from contacts and connecting wires, gate oxide ( $\text{SiO}_2$  or  $\text{Al}_2\text{O}_3$ ), gate metal, buried insulator and Si substrate. The thermal resistance of the substrate is calculated with the linear approximation for thermal diffusion, which basically associates to each device a conic dissipation region.

The impact of various device parameters was analyzed: nature and thickness of the BOX, gate length (from 10 to 80 nm), film thickness (down to 5 nm), nature of gate insulator (with 2 nm equivalent oxide thickness), etc. Figure 1 confirms that the buried insulator plays the key role in heat dissipation, as compared to contributions from the front-gate stack or S/D terminals.

The total heat dissipation degrades in short channels due to the narrower path of heat fluxes through the gate and BOX. Figure 2 provides a full support to our approach: switching from buried  $\text{SiO}_2$  to  $\text{Al}_2\text{O}_3$ , improves substantially the thermal conductance. By comparison the change in gate dielectrics is marginally beneficial. The advantage of using buried  $\text{Al}_2\text{O}_3$  is accentuated in

aggressively scaled MOSFETs: directly, because the channel is shorter (Fig. 1) and, indirectly, because short-channels require thinner films which enhance self-heating (Fig. 2). Most of the heat being evacuated through the BOX, it is clear that the modern trend of utilizing thinner buried insulators improves the thermal budget.

Our thermal resistance model can serve to evaluate self-heating. For a fixed power dissipation, the relation between thermal conductance and temperature rise is direct. For a fixed bias, the calculations are more complex because self-heating reduces dynamically the drain current and power.

In conclusion, an SOI-like structure with alumina as buried insulator is extremely attractive, at least for improved thermal dissipation. To validate this new concept, we discuss the process flow, experimental data, and simulation results.

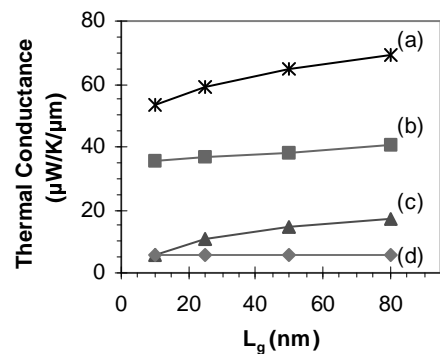


Fig.1. Gate-length dependence of the thermal conductances of various contributing regions: (a) full transistor, (b) BOX ( $\text{Al}_2\text{O}_3$ ) and substrate, (c) gate with  $\text{Al}_2\text{O}_3$  stack, and (d) source.

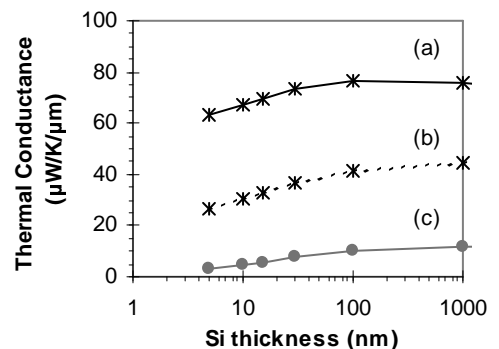


Fig.2. Influence of Si-film thickness for gate-oxide/BOX combinations on the thermal conductance of: (a) full transistor ( $\text{Al}_2\text{O}_3/\text{Al}_2\text{O}_3$ ), (b) full transistor ( $\text{SiO}_2/\text{SiO}_2$ ), and (c) source or drain.

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