Ultralow-Power FD-SOI LSI Design for Future Mobile Systems

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The use of mobile systems with communication functions has expanded rapidly in recent years. Considering the coming era of ubiquitous or pervasive networking computing, the number and variety of mobile units is expected to increase much more. For such equipment, further miniaturization and longer battery life are required and, eventually, batteryless mobile systems are foreseen. Maintenance-free systems without a battery are desired as terminals for ubiquitous networking computing. Ultralow-power design is essential for meeting these requirements. For CMOS LSIs, which are the key components of mobile systems, lowering supply voltage and using SOI devices are the most effective design approaches for reducing power dissipation. We have developed multi-threshold (MT) CMOS/SOI circuits [1] [2], which are suitable for operation at supply voltages as low as 0.5 V. And we have expanded the MTCMOS/SOI circuit technology to LSIs in mobile equipment. So far, some digital and analog components, such as a CPU, a memory, an analog/RF circuit, and a DC-DC converter for an ultralow-power mobile system have been developed [3].

The relationship between the target application and LSI performance is shown in Fig. 1. SOI devices are already being used in ultrahigh-speed and micro-watt applications like servers and watches, but, not in wireless mobile equipment like PDAs. Their power dissipation is still from 100 mW to 1 W. Our aim was to make the power dissipation about two orders of magnitude less than that of conventional LSIs, and our target application is set a short-range wireless system. Ultralow-power LSIs with power dissipation from 1 to 10 mW should open the way to batteryless mobile systems. A block diagram of an ultralow-power wireless system is shown in Fig. 2. Applying 0.5-V digital LSIs and 0.5~1-V analog/RF LSIs, we set a power dissipation goal of about 1 mW for the digital components and 10 mW for the analog/RF ones.

In making ultralow-voltage and ultralow-power LSIs, suppressing the leakage current is the main issue. There are two key technologies for doing so. One is fully-depleted (FD) SOI technology and the other is MTCMOS circuit technology [1]. Since FD-SOI MOSFETs have a steep subthreshold swing close to the ideal value of 60 mV/decade and are three-terminal devices, they make it possible to reduce the threshold voltage without any leakage current. An MTCMOS/SOI circuit [2] is shown in Fig. 3. The medium-Vth CMOS blocks are used for noncritical paths, thereby suppressing the leakage current in the active mode. And the high-Vth power-switch transistor reduces the leakage current in the sleep mode. For analog/RF circuits, FD-SOI devices have some advantages, in addition to those for digital circuits. One is that the primary measures of analog performance, namely, gm, fT, and fmax, improve at a low supply voltage. Another is that FD-SOI devices have good immunity to substrate noise due to the isolation provided by the buried oxide layer and to the high-resistivity substrate. This type of substrate also improves the performance of passive elements, like the Q-values of inductors.

To verify the effectiveness of our ultrallow-voltage MTCMOS/SOI circuits, we fabricated a batteryless short-range wireless system [4]. A photograph of the system is shown in Fig. 4. The system consists of a transmitter and a receiver that, owing to the use of our ultralow-voltage SOI circuit technology in the 1-V RF circuit, a 0.5-V 8-bit CPU, and an SC-type DC-DC converter, operate with by spring drive and on a solar cell, respectively. Wireless transmission from a distance of ten meters was successfully performed without a battery.

Acknowledgment

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References

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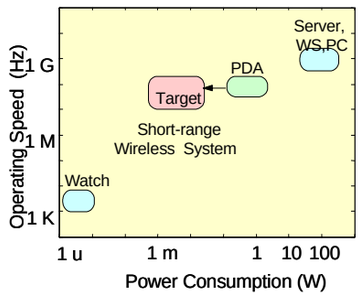

Fig.1 Target application and LSI performance.

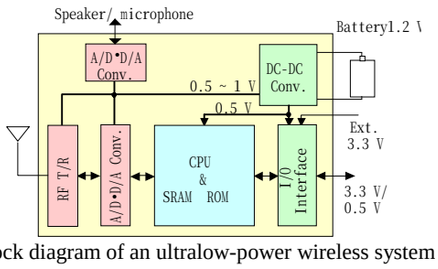

Fig.2 Block diagram of an ultralow-power wireless system

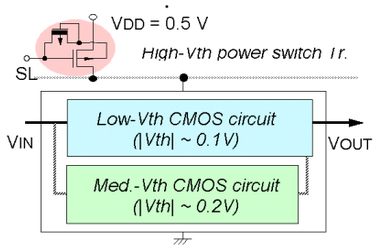

Fig.3 MTCMOS/SOI circuit scheme.

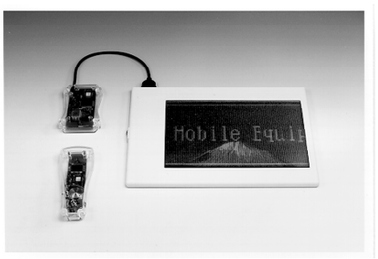

Fig.4 Batteryless short-range wireless system.