Strained Si/SiGe Channels: A New Performance Advantage for PD/SOI CMOS

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Introduction

Strained Si channels, resulting from the lattice mismatch of an underlying relaxed $Si_{1-x}Ge_x$ layer, have been shown to yield improved carrier-transport properties, including high-field velocity as well as mobility [1]. The improvement, dependent on the Ge content x, comes with a narrowed energy bandgap [2], which yields a reduced threshold voltage (V_t) for the heterostructure MOSFET. Hence, the CMOS performance enhancement afforded by strained channels tends to be limited when V_t and off-state current (I_{off}) are properly controlled. Further, the narrowed bandgap and the higher permittivity of SiGe imply increased source/drain junction capacitance, which also limits the performance. Although most of the exploratory work on strained Si/SiGe channels has been done with bulk-Si MOSFETs, the latter limitation implies a new performance advantage for floating-body PD/SOI CMOS when strained Si/SiGe channels are incorporated (SSOI) [3]. In this paper, we use our process/physics-based compact model, UFPDB [4], which is unified for bulk-Si and PD/SOI MOSFETs, to project, versus x, the speed-performance of scaled SSOI CMOS, and to assess its new advantage over the bulk-Si counterpart.

UFPDB and Its Strained Si/SiGe Option

In contrast to more common empirical compact models, UFPDB is process/physics-based, having a small set of parameters that relate directly to the MOSFET structure and the pertinent device physics. The parameters hence can be well estimated without copious data sets of measured electrical device characteristics, and the model can be predictive. For the analysis reported herein, we have upgraded UFPDB with a strained-Si/SiGe option [4]. One new parameter (GEX, which is also a flag for the option) is x, which is used internally to define the bandgap narrowing in the channel as [2]

$$\Delta E_g = E_{g(Si)} - E_{g(Si/SiGe)} = 0.4x \text{ (eV)}. \qquad (1)$$

The reduced V_t is then implicitly predicted. The increased source/drain junction capacitance is defined by reducing the potential barrier by ΔE_g and increasing the permittivity based on a simple interpolation between Si and Ge, $\varepsilon_x = (11.7 + 4.6x)\varepsilon_0$, in the model expressions for junction depletion charge. These modifications are done for the peripheral charge components, defined by the halo doping density, and, for the bulk-Si mode, for the areal components, defined by the well/substrate doping density. For the SOI mode, with floating-body (FB) effects controlled by several carrier recombination-generation mechanisms [4], the reduced bandgap, which also defines an increased intrinsic carrier density, is further used to define increased junction recombination-generation rates. Finally for the Si/SiGe option, four other model parameters that define carrier mobility, velocity saturation, and velocity overshoot depend on x, and must be specified on the model card accordingly. These parameters, for example, define the important differences between the mobility enhancements for electrons and holes [1], and the significances of velocity overshoot for electrons and holes in strained Si [5].

Analysis

We consider PD/SOI CMOS scaled to near its limit. Based on 2D numerical device simulations, we first calibrated UFPDB-2.5 to representative L_{gate} = 60nm (L_{eff} = 50nm) bulk-Si CMOS devices. The source/drain areas were defined based on a 6λ design rule for length, with λ = 65nm. The PD/SOI counterpart devices were then defined directly, replacing the well/substrate with a thick back oxide. The source/drain-junction recombination parameters were set based on measurements of FB effects in scaled test PD/SOI devices. Based on the control devices, strained $Si/Si_{1-x}Ge_x$-channel devices, with x ranging from 0.10 to 0.50, were then defined with UFPDB-2.5 by specifying GEX as x, and defining the other four x-dependent parameters properly for the nMOSFETs and the pMOSFETs [5].

UFPDB-predicted current-voltage characteristics of the control and strained Si/SiGe devices (at a typical elevated operating temperature) then revealed the V_t adjustments in the latter needed for equal I_{off}, which were effected by increasing the channel doping density (parameter NBL), implying a reduction in low-field mobility (parameter UO) and increases in associated doping densities. We note that the FB effects at the elevated temperature were well controlled, and did not mandate any additional V_t increase.

To check the speed-performance enhancement afforded by the strained Si/SiGe-channel MOSFETs in the 60nm CMOS technologies, UDPDB/Spice3 was used to simulate 9-stage unloaded inverter-based ring oscillators at the elevated temperature with V_{DD} = 1.0V. We focus on (a) the optimal x, (b) the speed enhancement yielded by SSOI relative to PD/SOI CMOS, and (c) the added advantage of strained-Si channels in SOI CMOS relative to bulk-Si CMOS, for which our simulations reveal (a) ~0.20, (b) ~13%, and (c) ~8%, with the latter giving a ~36% total speed advantage for SSOI CMOS over the bulk-Si counterpart. Insightful explanations of these predictions will be given based on details of the device- and circuit-simulation results.

Acknowledgments

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References

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