Study of the Leakage Drain Current in Graded-Channel SOI nMOSFETs at High-Temperatures

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Recently, it was presented a new asymmetrical channel doping device known as Graded-Channel SOI nMOSFET (GC SOI) [1-2]. In this structure, the conventional threshold voltage ionic implantation is masked on the drain side, preserving the natural wafer doping level, and is performed only on the source side to define the target threshold voltage. Some previous works showed the GC SOI nMOSFETs potential use in analog circuits such as operational transconductance amplifiers [2] and current mirrors [3], due to its reduced drain output conductance associated to the transconductance increase.

In order to study the leakage drain current I_{DLeak} behavior in GC SOI nMOSFETs operating at high-temperatures (up to 300°C), it was necessary to extract the drain current as a function of the front gate voltage curves. This study was done initially using numerical bidimensional simulator MEDICI[4], where the channel length L is 4µm, the gate oxide, silicon film and the buried oxide thickness are t_{oxf} = 31nm, t_{Si} = 80nm and t_{oxb} = 390nm, respectively. The doping level near the source is Na_H=1E17cm^{-3} and in the region near the drain Na_L=1E15cm^{-3} (natural doping level).

To realize this work, some comparisons were done based in two conventional SOI nMOSFETs devices with L=2µm, where the gate oxide, silicon film and the buried oxide thickness are the same values used in the GC SOI nMOSFET and for Na = 1E17cm^{-3} and Na = 1E15cm^{-3}.

The leakage drain current I_{DLeak} in SOI nMOSFETs was extracted from the I_{DS} *vs.*V_{GF} curves (with the same drain bias) for the front gate voltage V_{GF} being equal to -3V, where the current almost independs on the V_{GF} bias (as showed in fig. 1) and for all temperature range analyzed.

Figure 1 shows the comparison between the drain current *vs.* front gate voltage curves for two conventional SOI devices and a GC SOI nMOSFET, operating at the same conditions (temperature and bias). It is possible to observe that the current level is higher in lower doping device, as expected due to the low threshold voltage. It can also seen that I_{DLeak} in GC SOI nMOSFET is similar to the conventional SOI MOSFET with Na=1E17cm^{-3}, showing that the leakage dominant behavior is governed by the high doped region.

Figure 2 shows I_{DLeak} behavior as a function of the temperature in conventional SOI and GC SOI nMOSFETs. From these results, it can be seen that when the temperature increases, I_{DLeak} increases similarly to the conventional SOI nMOSFETs [5]. For the GC SOI nMOSFET it is possible to see that I_{DLeak} level is quite similar to the conventional SOI nMOSFET, for Na=1E17cm^{-3} and for all temperature range. It also happens since the effective channel length in both devices is the same.

Analyzing I_{DLeak} behavior in GC SOI nMOSFETs, it can be observed that it depends strongly on the L_{LD} / L ratio, where I_{DLeak} increases when the low doping level region (L_{LD}) increases, as it can be seen in figure 3. It happens due to the effective channel length reduction (Leff ≅ L – L_{LD}) when L_{LD} increases [5].

As a conclusion, I_{DLeak} in GC SOI devices is dependent on low doped region length (for a fixed L) and high doped region concentration (Na_H).

References

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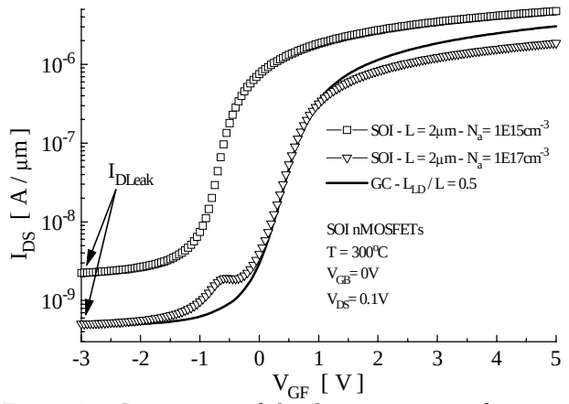

Figure 1 – Comparison of the drain current vs. front gate voltage curves between conventional SOI and GC SOI nMOSFETs at 300°C.

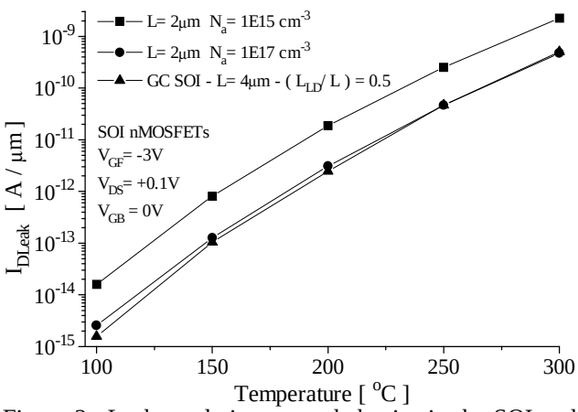

Figure 2 –Leakage drain current behavior in the SOI and GC SOI nMOSFETs as a function of the temperature.

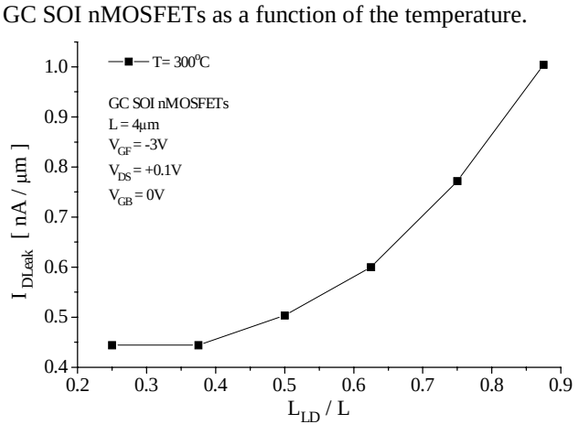

Figure 3 – The leakage drain current dependence of the L_{LD} / L ratio in GC SOI nMOSFETs operating at 300°C.