# Modeling of Coulomb Scattering of Electrons in Ultrathin Symmetrical DG SOI Transistor

J. Walczak, B. Majkusiak Institute of Microelectronics and Optoelectronics Warsaw University of Technology Koszykowa 75, 00-662 Warsaw, Poland

## 1. INTRODUCTION

Coulomb scattering is one of the most severe factors limiting channel mobility and has been widely studied for MOSFETs (1), (2). Due to adjacent media of different dielectric constants forming a transistor, the scattering potential is affected by image charges induced by scatterers. An image charge model for ultrathin DG SOI devices is developed in this paper and applied to investigate the dopant ions limited electron mobility.

# 2. THEORY

Double Gate Silicon-On-Insulator transistors, which are a promising alternative to MOSFETs, comprise an active silicon layer as a channel, sandwiched between two oxide layers covered by a gate material (3). Here we investigate a symmetrically operated n-channel device with Al gates (Fig. 1). In MOSFET's Coulomb scattering theory, semi-infinite media (SiO<sub>2</sub>-Si) are often assumed, hence one only image of a point charge Q located in semiconductor is included. In SOI devices another interface arises and a given semiconductor thickness is imposed. Therefore, more image charges are seen in the semiconductor, which, for negligibly thick gate oxide, may be determined as in Fig. 2 by alternating reflections around the both interfaces. The total induced image potential is then higher than that for a MOSFET. However, in ultrathin devices both the oxide and the active layers are of nanometric scale so the gate is supposed to affect the total image potential. This can be determined by superposition of image charge solution for the three media of interest (4) and reflections around Si-SiO<sub>2</sub> interfaces, obtaining a series of positive and negative image charges (Fig. 3).

Having the total image charge determined the selfconsistent procedure is employed to determine energy levels, electron scattering rates with screening included and Coulomb mobility within the relaxation time approximation. Fig. 4 shows the calculated impurity ions limited electron mobility vs. effective transverse field for DG SOI of different semiconductor thickness (15 - 2 nm) and for N-MOSFET whereas Fig. 5 shows the mobility for different oxide thicknesses. Curves denoted as "conv." refer to a simple "one real - one image" charge model, symbol "∞" corresponds to semi-infinite oxide layer for DG SOI.

#### 3. CONCLUSIONS

Calculated electron mobilities for DG SOI are higher than for MOSFET, increasing with decreasing  $t_s$  value. It results from higher and higher relative electron occupation of the lowest energy level of the smaller conductivity electron mass with thinning the DG SOI silicon layer. Furthermore, it can be seen that  $\mu_{Coul}$  increases slightly for oxides below ca. 3 nm, this being an effect of screening the scattering centers by the metal gate.

### ACKNOWLEDGMENTS

The work supported by KBN Poland, Grant 4T11B03523.

# REFERENCES

- 1. T. Ando et al., Rev. Mod. Phys. 54, 437 (1982).
- 2. F. Gámiz et al., J. Appl. Phys. 75, 924 (1994).
- 3. F. Balestra et al., IEEE El. Dev. Lett. 8, 410 (1987).

 M. Kleefstra and G.C. Herman, J. Appl. Phys. 51, 4923 (1980).



Fig. 1. A simplified cross-section of a DG SOI transistor.







Fig. 3. Image charges seen in DG SOI device for  $t_{ox} \propto t_s$ .



Fig. 4. Coulomb electron mobility for different  $t_s$ .



Fig. 5. Coulomb electron mobility for different  $t_{ox}$ .