Analysis of HALO Implant Influence on the Self-Heating and Self-Heating Enhanced Impact Ionization on 0.13 mm Floating-Body Partially-Depleted SOI MOSFET at Low Temperature

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Introduction

The reduction of the device dimensions makes necessary the use of HALO implant to control the leakage current and subthreshold slope to adequate values. The use of SOI floating-body (FB) partially depleted (PD) nMOSFETs has already shown better speed/power consumption performance if compared to the bulk counterpart[1]. The problem regarding the FB in the well known kink effect that degrades the output conductance (g_D) in saturation. Self-heating occurrence phenomenon increase the amount of impact ionization current by locally providing a source for carrier heating, reducing the mobility[2]. In addition to this effect, the use of HALO implant increase the doping level both at the source/drain junctions, elevating the barrier for the holes generated by impact ionization[3]. The combination of these two phenomena maybe favorable to oversize the degradation, mainly at low temperatures.

The goal of this study is to verify the impact of HALO implant on self-heating and self-heating enhanced impact ionization current both at room temperature and at 90 K for 0.13 μ m PD technology. Two dimensional simulations[4] and experimental results are used to support the analysis.

Device fabrication

The 0.13µm PD transistors were fabricated using standard UNIBOND wafers with a film thickness of 200 nm and a buried oxide thickness of 400 nm. The PELOX technique has been used to isolate the device active regions. A 2.5 nm thick post-annealed nitrided oxide (NO) is grown and a 150 nm polysilicon layer is deposited. The final silicon film thickness is 100 nm. After the gate definition, low energy ion implantation of arsenic is performed for the formation of shallow source/drain extensions followed by the HALO angled implants to control the short-channel characteristics. Devices without HALO and with a 3 x 10^{13} cm⁻² BF₂ at 65 keV HALO have been fabricated.

Results and Discussion

In order to characterize the self-heating dependence on the HALO concentration and access the impact ionization current (I.I.) to get a physical insight, the doping level of the two-dimensional simulations has been adjusted to fit the experimental data. Coupled solutions including the lattice temperature (LT) model equations were made to include the heating effect. Figure 1 presents the simulated I.I. and the ratio between I.I. over the drain current (I_{DS}) *versus* gate voltage overdrive (V_{GT}=V_{GS}-V_T), for a fixed drain-to-source (V_{DS}) voltage of 1.2 V, of 0.13 µm FB PD nMOSFETs with and without HALO implant at room temperature. It is clear from the simulations that the HALO presence tends to result in larger impact ionization current.



Figure 1 – Simulated I.I. and $II/I_{DS} \times V_{GF}$ for HALO and non-HALO devices.

Based in the simulation results one can see that the selfheating causes an increase in the impact ionization current which agree to [2]. In addition, the HALO implant tends to make this problem harder at large gate voltages.

Figure 2 plots the measured I_{DS} versus drain voltage (V_{DS}) extracted for low V_{GT} for the studied devices at 90 K. The HALO influence can be noted on the self-heating appearance (negative g_D) at V_{GT} of 200 mV and 400 mV while in the non-HALO structure this effect it is not observed. In addition, the reduction of the temperature increase the barrier for the holes generated by I.I. and a very pronounced kink effect is observed in the HALO transistor and only a soft kink effect happens in the device without the HALO implant.



On the other hand, in order to minimize the generated I.I., the V_{GT} has been increased to 1.4 V, as presented in figure 3 which plots the resulting g_D versus V_{DS} . Also in this case, the HALO device present negative values for g_D which is not observed in the devices without HALO implantation.

References

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