Temperature and magnetic field dependence of the carrier mobility in SOI wafers by the pseudo-MOSFET method

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The pseudo-MOS transistor (Ψ-MOSFET) is a useful non-destructive technique to evaluate Silicon on Insulator (SOI) wafers before any processing (1,2). From the drain current versus gate voltage characteristics I_D (V_G), parameters such as the threshold voltage V_T, flat-band voltage V_{FB}, electron or hole mobility μ_e, μ_h, as well as interface trap density D_{it} can be derived. A way to determine μ_e and μ_h is from the slope of the linear curve $I_D/\sqrt{g_m}$ versus V_G, where g_m is the transconductance. In this paper, we present two novel extensions of the Ψ-MOSFET technique, in the temperature and magnetic field domains.

We measured the above parameters, in particular the electron and hole mobilities, as a function of temperature T on 10 × 10 mm^2 pieces of UNIBOND wafers (200-nm-thick SOI, 400-nm-thick BOX) with etched edges to prevent leakage. The residual doping of the *p*-type Si(100) layer is less than 2–5 × 10^{15} cm^{-3}. From T = 10 K up to 400 K, I_D (V_G) was measured with a custom-made sample holder, using two spring-loaded tips for source and drain contacts and silver paint for the back gate contact. The sample was mounted in the insert of a He-cryostat with magnetic field capability up to H = 7 T. For calibration of our system, similar Ψ-MOSFET data were taken at 300 K on a four-point probe station with adjustable needle loading. The high-temperature dependence of the mobility was measured up to 800 K in a UHV chamber using patterned structures with Al contacts bonded with Pt wires.

As shown in Fig. 1, the electron mobility increases continuously from 110 cm^2/Vs at 700 K up to about 2300 cm^2/Vs at 75 K, where it reaches a peak value before falling rapidly to 1220 cm^2/Vs at 20 K. The hole mobility follows a similar trend, rising from 60 cm^2/Vs at 650 K to a maximum of 550 cm^2/Vs at 100 K. The observed decrease of μ_h (T) below 250 K might be related to an enhanced sensitivity of the accumulation channel to a larger needle contact resistance.

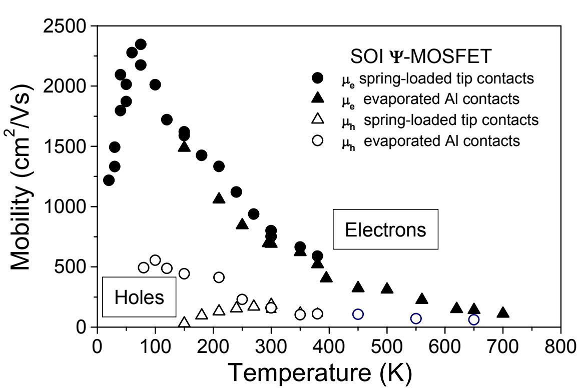

Fig. 1: Temperature dependence of the electron and the hole mobility of *p*-type SOI wafer.

The analysis of $\mu_e(T)$ displays three power-law regimes with exponents close to 0.5 below 75 K, –0.45 in the intermediate range (75–250 K), and –1.5 at higher temperatures. Discussion is made with respect to the different carrier scattering mechanisms as a function of temperature. The magnetic field dependence of the mobility has also been measured at low temperature. At 75 K, $\mu_e(H)$ decreases by 60% at 5 T, following a $\mu(H) = \mu(0) / (1 + \alpha H^2)$ law, in agreement with the typical magnetoresistance behavior (Fig. 2).

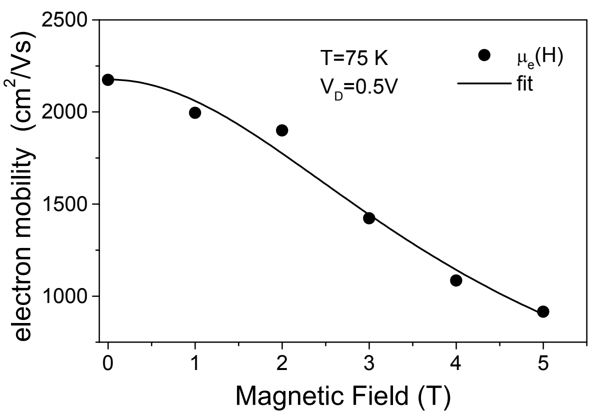

Fig. 2: Field dependence of the electron mobility at 75 K

In conclusion, measurements at variable temperatures and magnetic fields allow the extraction of more detailed information with the Ψ-MOSFET technique. The prevailing scattering mechanisms and the roles of interface quality and doping are key aspects in SOI material optimization.

REFERENCES

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