# Steady-state characterization of partially depleted SOI CMOS Gates

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## I. Introduction

History effects are an important constraint for digital circuit design using partially depleted SOI substrate [1]. In most cases, gate delay evaluation of SOI cells is restricted to a "2 points characterization", that means a first and second switch analysis [2]. But recently, methods for steady-state determination have appeared, in which reaching the dynamic equilibrium does not require thousands of electrical simulation cycles [3][4]. 3 points characterization are then possible, allowing a better hysteresis characterization. We propose in this paper a few observations of basic cells steady-state behavior. The simulations are achieved with the LETISOI model.

## II.Steady state and frequency

Compared to a first and second switch characterization, a steady-state delays determination must account for supplementary parameters, that are frequency and duty-cycle of the applied signal.

We show in figure 1 the variation of pull-up and pull-down steady-state delays for a single inverter simulated with a 0.25µm technology. For frequencies under 1 MHz, a small dependency of delays on frequency shows that the recombination-generation phenomena have an impact on steady-state charge when the high and low stages are long enough. But for higher frequencies and up to the maximal circuit operation frequency, the steady-state delays become independent of frequency. It evidences that the charge variation depends essentially on charge coupling during the edges.

The figure 2 presents the steady-state delay of a rising edge, but for a 0.12µm PD technology. In this case, the delay depends on frequency, which is due to the gate current influence during the high and low stages. Gate current arises effectively for reduced oxide thickness of advanced technology.. If we cancel the LETISOI model gate current parameters, the frequency dependency is also reduced (see fig.2).

## III. Steady state and duty-cycle

The duty-cycle is susceptible to vary along a gates chain due to the different rising and falling edges delays in the successive gates. Thus, the steady-state variation with duty-cycle is important for design characterization. The table 1 shows the body potentials of NMOS and PMOS transistors in a single inverter for 2 periods duration. For the short period, the delays do not depend on duty-cycle, whereas for the long period, it impacts strongly the both FETs body voltages. It confirms that the charge diffusion is negligible in front of capacitive coupling in the body charge equilibrium process at classical frequency ranges.

## IV. Steady state and load capacitances

For a 200ps input slope, we have simulated the steady-state body to source potentials of both inverter transistors as a function of the load capacitance. The strong dependency can be observed on figure 3. But it is known that the history effects decrease proportionally when the load capacitances and consequently the delays increase.

For a gate characterization, it is then possible to extract the steady-state body voltages for only one small load capacitance and to use these values to measure the steady-state delays in all the load capacitance range.

## V. Conclusion

Now the steady-state may easily become a corner point for delay characterization of CMOS cells, it is important to estimate the steady-state behavior under different influences, signal frequency, input slopes and temperature (Other points will be developed in the final paper version).

## VI. References

[1] M.Pellela et al., "Hysteresis in FB PDSOI Circuits", VLSI-TSA, 1999.

[2] F. Assaderaghi et al., "History Dependence of NFD Digital SOI Circuits", Symp. On VLSI, pp. 121, 1996.

[3] M.R. Casu, P. Flatresse, "History Effect Characterization in PDSOI CMOS Gates", 2002 SOI Conf

[4] I. Aller et al., "Detailed Analysis of the Gate Variability in PDSOI CMOS Circuits",1999 SOI Conf.

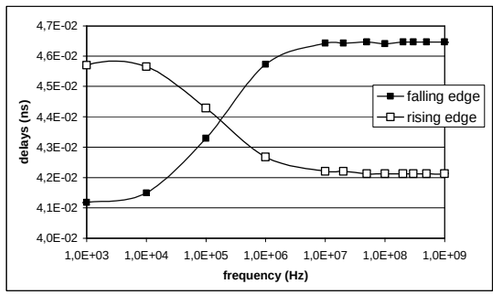


*Fig. 1 : Rising and falling edge delays as a function of frequency (input slope : 200ps, load capacitances :15 fF)*

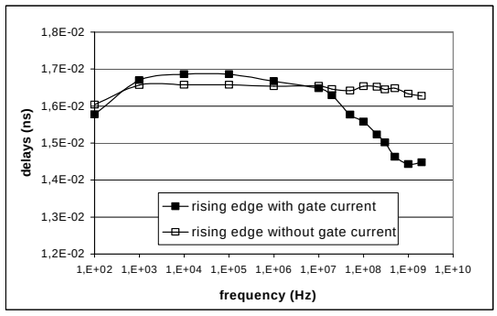


*Fig. 2 : Rising edge delays as a function of frequency (input slope : 200ps, load capacitances :15 fF) for a 0.12 µm technology with and without gate current*

| Period | 100 ns | | | 10 ms | | |
|---|---|---|---|---|---|---|
| Duty Cycle | 2% | 50% | 98% | 2% | 50% | 98% |
| Vb (NMOS) | 0.193 | 0.193 | 0.193 | 0.207 | 0.130 | 0.102 |
| Vb (PMOS) | 1.663 | 1.656 | 1.649 | 1.684 | 1.585 | 1.552 |

*Table 1 : Body potential of both transistors in an inverter as a function of duty-cycle for 2 periods*

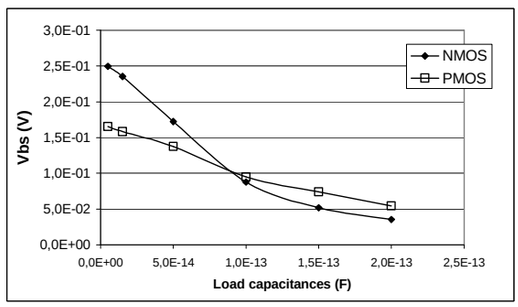


*Fig.3 : Steady-state body potentials of NMOS and PMOS of an inverter as a function of load capacitance*