Emerging Silicon-On-Nothing (SON) Devices Integration

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Extremely thin (nanometric) films of mono-crystalline Silicon on insulator are widely recognized for their potential for end-of-roadmap CMOS transistors. In contrast with any other SOI technology, in the SON process, the silicon film and buried insulator, both of nanometric scale, are defined by epitaxy on a bulk substrate.

Therefore, the SON process opens access to extremely thin films (the Silicon channel as well as the BOX) at the same time offering the thickness control as fine as the resolution of the epi process (less than 1nm). In this paper we present why the very thin layers in the SON transistor allow high control of the short channel effects due to the suppression of any electrostatic lateral coupling (in the channel and in the BOX) and allow in this way excellent electrical performances.
Electrical results will be presented presented, showing functional SON transistors with gate length down to 38nm, with a conduction channel thickness as thin as 9nm (see **fig.1**). We measured in particular a large improvement in terms of SCE (Short Channel Effects) control due to the thin conduction channel and to the ground plane effect.
As the silicon conduction film thickness becomes defined by epitaxy in the SON process, transistors with conduction channel down to 5nm have been performed, see **fig.2**.

It is also demonstrated that SON is better suited than bulk for accepting a metallic gate for low-voltage operation due to the intrinsic low threshold voltage of such thin films.
In this work, we will present mid-gap $CoSi_2$ metal gate by total gate silicidation on SON transistors with Si-conduction channel thickness down to 5nm. Due to its architecture and to the continuity between SD areas and the bulk, SON transistors allow deep silicidation process down to the gate oxide, meaning that no more polysilicon is left. SON PMOS devices were performed with 55nm $CoSi_2$ gate length with 5nm of Si-channel thickness, **fig.3**.

Finally, we will show SON-Ion/Ioff performances projected onto the 2001 ITRS CMOS roadmap. It will be shown that the performances missing to bulk with respect to ITRS specifications, can be totally recovered by SON. Consequently, we will show how SON with totally silicided gate are capable to realize the entire LP ITRS roadmap.

References

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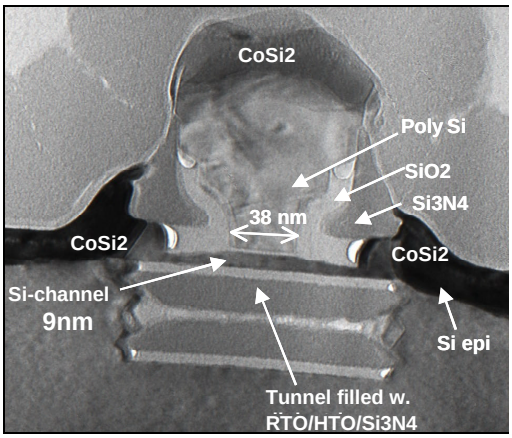
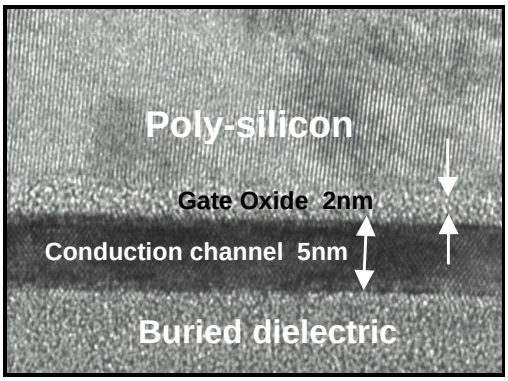
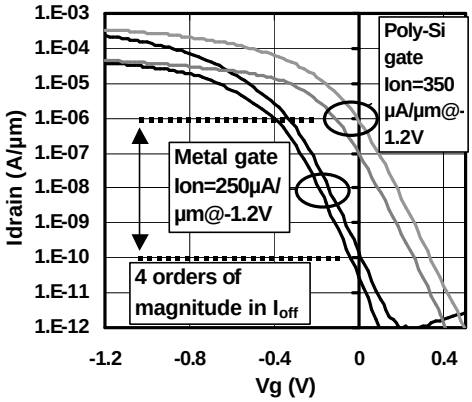


1. *38nm SON PMOS transistor with 9nm of Si-conduction channel. Junctions are silicided with $CoSi_2$.*



2. *HRTEM picture showing the thickness of the Si-channel. Measured T_{Si}=5nm, with perfect top and bottom interfaces.*



3. *Comparison of Log-Id(Vg) curves of 55nm SON devices with poly-Si gate and $CoSi_2$ gate. Due to the very thin depletion depth (T_{Si}=5nm), the low threshold voltage of the transistor with poly-Si gate leads to high I_{off} that can be reduced by 4 orders by adjusting V_{th} with the mid-gap gate. Tox=20Å*