Fully Depleted SOI Process and Device Technology for Digital and RF Application

F. Ichikawa, Y. Nagatomo, N. Hirashita,
Y. Katakura, S. Itoh, and H. Matsuhashi
Oki Electric Industry Co. Ltd., Silicon Solutions Company, System LSI Research Division,
Higashi-Asakawa, Hachioji, Tokyo 193-8550, Japan

1. Introduction

Fully-depleted (FD) SOI-CMOS technology allows the threshold voltage low due to its good subthreshold characteristics, resulting in the high performance of low voltage digital circuits. The SOI technology is now penetrating the commercial market in digital logic circuits. [1] Our 0.35 and 0.2 μm FD-SOI technology had been already applied to custom LSIs. Also the rapid growth in digital wireless communications has brought an increasing demand for high-performance radio-frequency (RF) circuits in low-cost technologies. A major challenge is to realize CMOS single chip. This paper presents currently applied status of low voltage digital logic and RF FD-SOI devices as well as their mass productivity.

2. Low power application

Figure 1 shows a comparison of bulk and FD-SOI device performance for 32bit RISC processor using with the same layout pattern. The FD-SOI CMOS devices exhibit the same performance at 1.5V operation as the bulk CMOS at 2.5V operation, indicating power reduction of 64%.

3. RF device application

Characteristic features of high frequency operation at V_{ds}=1V for 0.15 μm FD-SOI FETs are summarized in Table 1, which indicates that RF devices of 10GHz range band can be realized even at low operation voltage. Figure 2 shows the measured inductance and Q values of the spiral inductors fabricated on the high- and low-resistivity SOI substrates of 1kΩ-cm and 20-30Ω-cm, respectively. The Q values, superior to the bulk devices, are further improved 20% by using the high-resistivity SOI substrates. Low noise amplifier (LNA), voltage-controlled oscillator (VCO), and single-pole double-throw switch (SPDT-SW) were successfully fabricated and they exhibited higher gain, lower noise figure, and reduced insertion loss at GHz frequency for high-resistivity SOI substrates. A comparison of crosstalk figure, S21 transmission parameter in dB, between the bulk and FD-SOI CMOS is shown as a function of frequency in Fig. 3. Crosstalk noise tolerance of FD-SOI CMOS is confirmed to be improved more than 20dB over wide range of high frequency operation to compare bulk CMOS since the SOI devices are completely isolated from the substrate. [2] The reduction of crosstalk, therefore, has a big deal over bulk CMOS when digital and analog/RF circuits are integrated together on single chip.

4. Conclusion

We have demonstrated suitable applicability of FD-SOI devices for low power digital and RF usages for wireless communication as well as realizing their single chip.

References

1) D. Schepis et al., IEDM Tech. Dig., 1997, p.587.
2) J-P. Raskin et al., IEEE T-ED **44** (12), 2252 (1997).

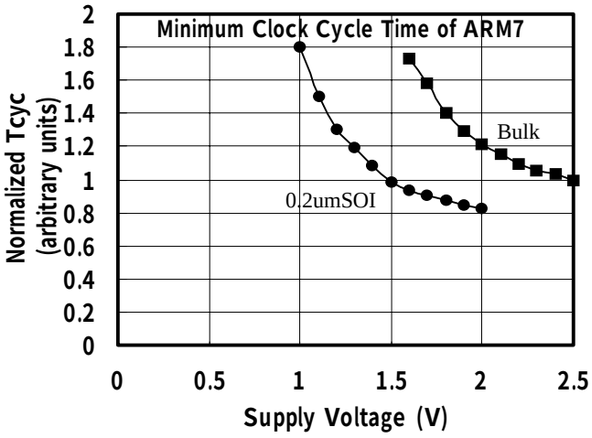

Fig. 1. A comparison of bulk and FD-SOI device performance for 32bit RISC processor.

Table 1. 0.15μm FD-SOI high-frequency characteristics.

	NMOS	PMOS
f_T	59GHz @V_{DS}=1.0V	29GHz @V_{DS}=1.0V
f_{max}	61GHz @V_{DS}=1.0V	37GHz @V_{DS}=1.0V

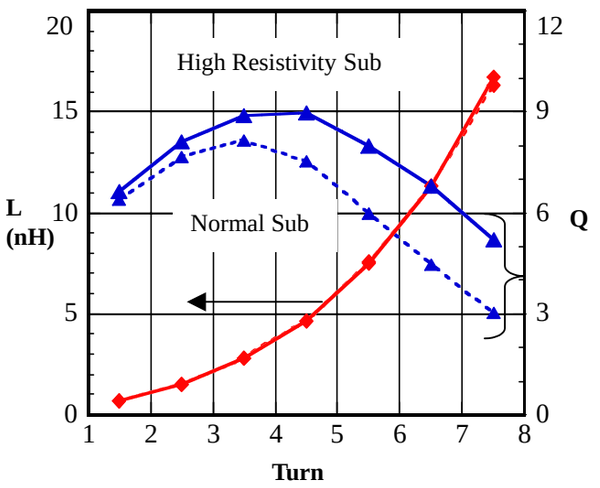

Fig. 2. The measured inductance and Q values of the spiral inductors fabricated on the high- and low-resistivity SOI substrates.

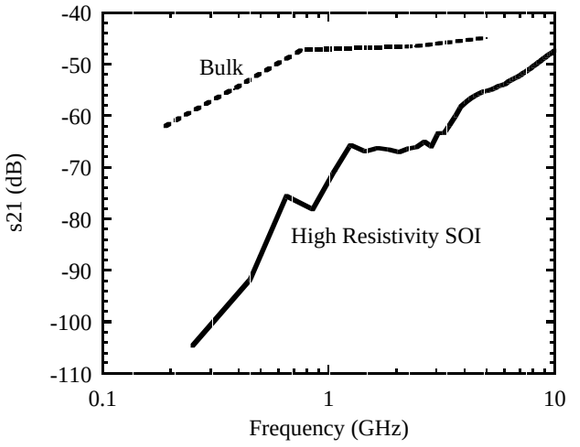

Fig. 3. A comparison of crosstalk figure between the bulk and FD-SOI CMOS devices.