A Novel Hot Wall Furnace-Based RTP System With Sequenced Hydrogen And Wet-Hydrogen Ambient Gases For Advanced Dielectric Applications: Processing And Characterization

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The processing of silicon-based CMOS device structures using hydrogen (H_2) and water vapor (H_2O) at elevated temperatures is of great importance for the repair of damaged gate oxides around tungsten (W) gate electrodes due to ion implantation or etching, high-quality thermal oxide growth, high-K gate dielectric growth and the corner rounding of shallow trench isolation (STI) etc. By integrating a new proprietary movable small-volume quartz reactor into a commercial single-wafer hot-wall rapid thermal processing furnace (Summit^{TM} RTP, Axcelis Technologies), the excellent thermal performance inherently associated with a large-volume hot-wall furnace is preserved while the effective gas volume around a wafer under processing has been reduced to less than three liters. Thus, real-time fast (<15 seconds) gas switching synchronized with wafer temperature has been realized so that multiple rapid thermal processing steps involving the sequential use of nitrogen, hydrogen, water vapor and their mixtures is realized in a single processing cycle. Water vapor diluted in hydrogen is quantitatively generated with a catalytic reactor.

In this presentation, we shall report our latest processing and characterization results on three important rapid thermal processes: (1) hydrogen anneal of Si(100) wafers and SiO_2 ultra-thin films , (2) Si oxide growth using wet-hydrogen (H_2O+H_2), and (3) the selective oxidation of Si in the presence of W using wet-hydrogen. Multiple analytical methods such as quadrupole mass spectrometry (QMS), optical ellipsometry, sheet resistance measurement, Auger electron spectroscopy (AES), and X-ray photoemission spectroscopy (XPS) have been used to chemically characterize ambient gas composition, Si(100) and $W/SiO_2/Si(100)$ wafers processed in hydrogen and wet-hydrogen at elevated temperatures (900°C-1150°C). The effects of high-temperature processing in hydrogen and wet-hydrogen on silicon oxide electrical properties have been systematically studied using a powerful non-contact Corona-Oxide-Semiconductor metrology tool (FAaST 330, SDI).

Hydrogen precleaning of Si(100) substrates is a critical process prior to the rapid thermal chemical vapor deposition (RTCVD) of epitaxial silicon. The removal of native oxide layer from Si(100) (dia.=200 mm) wafers has been successfully demonstrated using a sequenced nitrogen-hydrogen-nitrogen gas ambient at the atmospheric pressure. After a ~1150°C hydrogen anneal for 60 seconds, the averaged optical thickness over a Si(100) wafer decreased from 7.8±0.4 Å to 1.2±0.3 Å, indicating the native oxide has been successfully removed. Our interface trap density (D_{it}) spectroscopic measurements using the corona-oxide-semiconductor technique show that the hydrogen anneal of ultra-thin $SiO_2/Si(100)$ films at ~1100°C for 60 seconds not only eliminates the typical D_{it} peak associated with interfacial Si dangling bonds (i.e. electrically-active P_b defect centers), but also dramatically decreases the minimum interface trap density from $>3\times10^{11}$ $q\cdot eV^{-1}\cdot cm^{-2}$ to as low as $<3\times10^{10}$ $q\cdot eV^{-1}\cdot cm^{-2}$.

The wet-hydrogen oxidation rates of Si(100) have been measured for a wide range of processing conditions as defined by wafer temperature (950°C-1100°C), water vapor percentage (0% to 40%) and oxidation time (0-70 seconds). During wet-hydrogen oxidation, a Si(100) wafer is rapidly heated to a desired temperature while fast gas sequence is carried out to expose the wafer to (1) H_2 or N_2 for preheating, (2) H_2O+H_2 for Si oxidation and (3) H_2 or N_2 for cooling. Interface trap density spectral measurements indicate that $SiO_2/Si(100)$ films grown in wet-hydrogen have much lower interface trap densities than those grown in dry-oxygen and wet-oxygen. A within-wafer (WIW) oxide thickness uniformity of less than 1%(1σ) has been achieved.

The selective oxidation of Si versus W in the temperature range between 950ºC and 1100ºC has been successfully demonstrated with the single-wafer hot wall rapid thermal processor (RTP) when <25% water vapor diluted in hydrogen is used to process Si(100) and 500Å $W/1000Å$ $SiO_2/Si(100)$ blanket wafers. Sheet resistance, AES and XPS characterizations are used to extract electrical conductivity, elemental composition and oxidation state of the processed tungsten films. Particularly, continuous cycling of tungsten wafers 1,032 times through the RTP system has been carried out in a $16\%H_2O+84\%H_2$ gas ambient at 1060ºC for 30 seconds. This recipe results in an oxide layer of 56Å on Si(100). The tungsten wafer cycling test proves that problems associated with WO_3 condensation onto lamp-based RTP chamber walls are completely avoided when a small-volume quartz reactor is used inside a hot wall furnace-based RTP system for rapid gas switching.

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