PERFORMANCE ENHANCEMENTS FOR 50 NM PMOS BY ANGLED PAI AND F IMPLANTS

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A novel approach to decrease boron lateral diffusion for a given vertical PMOS drain extension (DE) junction depth (Xj) is presented. Retarding boron diffusion in the lateral direction permits scaling to narrow gate lengths without increasing the DE sheet resistance. Angled pre-amorphization implants (PAI) and angled fluorine implants (F) reduce PMOS gate-to-drain overlap capacitance (Cgd) by ~ 8% with no loss in drive current. The novel DE design is exploited to realize a significant drive current gain at the same Cgd and sub-threshold leakage.

Motivation: CMOS technology scaling dictates a systematic decrease in the DE Xj. In conventional scaling, implant and diffusion cycles are engineered to achieve a simultaneous reduction in lateral and vertical extent of the DE doping profiles. Simultaneous vertical and lateral Xj scaling or spacing the doping away from the gate with an offset spacer result in a higher sheet resistance in the DE region and a poorer saturation drive current. We propose to scale only the lateral extent of the junction by decreasing the lateral abruptness; and simulation results are used to illustrate the advantage.

Novel Approaches: In this paper, we show practical approaches to reduce lateral Xj while maintaining the same vertical doping profile: angled PAI and angled F. The two approaches are combined to create three experimental conditions that are illustrated and compared to the reference condition.

Device Results: The angled PAI and F were implanted in the PMOS drain extensions of the 50 nm gate length CMOS device with a nitrided gate oxide, shallow trench isolation and cobalt silicide contacts. In each experiment, the new approach is compared against a reference PMOS DE, which has a 0o PAI and a 0o F + boron implant Figure 1 shows angled PAI reduced Cgd at Vg=0 by 8%; however, Cgd at Vg=Vdd did not change. Lower ratio of Cgd at Vg=0 to Cgd at Vg=Vdd for the angled PAI indicates a more abrupt lateral junction. This Cgd result proves that we have successfully reduced the lateral abruptness for the same vertical Xj by using an angled PAI. The identical Ion/Ioff slopes obtained prove that the MDD resistance was not changed by the angled PAI. The saturation threshold voltage demonstrates the better short channel immunity, which also results in less sub-threshold leakage at narrow gate lengths. Manufacturability is improved since this process decreases threshold voltage roll off with gate length. This advantage can be realized to increase the drive current for the same Cgd. Results from experiment 2 (figure 2), where the channel doping is decreased show that we get a 3% improvement in the drive current for the same Cgd. Implants through amorphous layers channel less; therefore, angled PAI decreases lateral channeling. Also, boron diffuses by an interstitial mediated mechanism. Crystal re-growth following an amorphization results in no net interstitials in the re-grown region. When the amorphization is carried out to a longer lateral extent than where the boron is implanted, additional interstitials are eliminated in the lateral direction. In experiment 3, angled fluorine implant is compared against the reference. Once again we see a reduction in Cgd at no cost in the drive current. Fluorine, when present in amorphized silicon retards boron diffusion [1]. Tsuprem4 decks tuned to the Secondary Ion mass spectrometry (SIMS) data were exercised to predict the decrease in lateral diffusion caused by angled F implants. Simulation results show a 4 nm decrease in lateral junction with an additional angled F implant and confirm retarding boron diffusion decreases the lateral abruptness. Hence, similar to the angled PAI implant case, angled F implanted DE profiles can be redesigned to realize Ion improvement at a given Cgd. No loss in gate oxide integrity or an increase in junction leakage was observed for either of the techniques.

Summary: The drive currents shown here are at VDD=-1.1 V. Tailoring the lateral profile by angled antimony and angled F was demonstrated to be advantageous. Angled PAI decreased the Cgd by 8% at the same drive current or improved the drive current by 3% for the same Cgd. Angled F decreased the Cgd by 6%.

Reference:

1) D.F. Downey, J.W. Chow, E. Ishida, K.S. Jones, Appl. Phys. Lett., 73, 1263 (1998) .

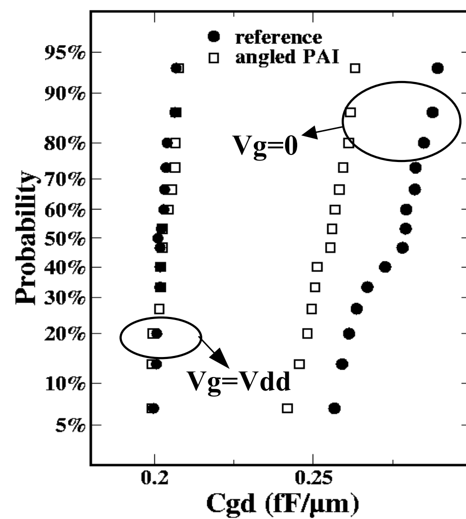

Fig.1 Normal Probability plot of drain to gate capacitance at zero and 1.1 volt biases for angled PAI (expt. 1). The lower lateral abruptness for the angled PAI is apparent from a decrease in Cgd at 0 V while similar at vdd.

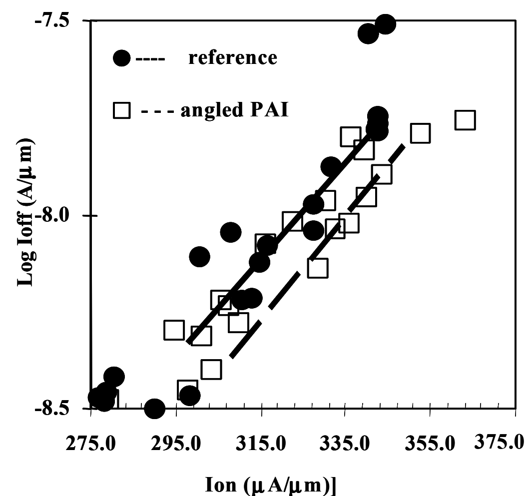

Fig.2 Ion/Ioff plot showing the drive current improvement by optimized angled PAI (expt. 2). The decrease in channel doping results in higher mobility.