SILICIDE SCALING : Co, Ni OR CoNi ?

A. Lauwers[1], J. A. Kittl[2], A. Akheyar[3], M. Van Dal[4], O. Chamirian[1], M. De Potter[1], R. Lindsay[1] and K. Maex[1]

[1] IMEC, 3001 Leuven, Belgium
[2] affiliate researcher at IMEC from Texas Instruments
[3] affiliate researcher at IMEC from Infineon
[4] Philips Research Leuven, Belgium

As scaling progresses beyond the 100 nm technology node, the source/drain junction depth has to be scaled well below 100 nm. To be compatible with the continuously decreasing junction depth, the silicide thickness has to be scaled down to lower the silicon consumption at the expense of a higher sheet resistance. In view of this trade-off it is crucial to minimize the silicide / silicon interface roughness. The Co-silicide / silicon interface roughness is known to be strongly determined by the nucleation of the Co-disilicide during the second step of Co-silicidation. Increasing the RTP2 temperature promotes the nucleation of Co-disilicide grains and is found to result in improved silicide interface roughness. Another way to promote the nucleation of the Co-disilicide phase is by alloying the Co film with Ni. The presence of Ni in the Co-film lowers the nucleation temperature of the Co-disilicide phase. This was verified by XRD for different Ni concentration as can be seen in Figure 1. Lower silicon consumption can also be achieved when Co-disilicide is replaced by Ni-monosilicide, which for the same silicide sheet resistance consumes 35% less silicon.

Moving on to the 65 nm node, gate lengths are scaled below 50 nm. It is observed that the sheet resistance of Co-silicided poly gates is increased drastically when the gatelength is reduced below 40 nm. (see Figure 2 for As doped gates) The degradation of the gate resistance for sub 40 nm gates seriously compromises the scalability of Co-silicide. It is studied whether the scalability can be improved by making use of Co alloyed with Ni. In addition, the performance of Ni-silicide for sub 40 nm poly gates is studied.

Ultrashallow, highly abrupt extension junctions with low sheet resistance are a requirement for advanced technology nodes. It is expected that meta-stable extension junctions obtained by Solid Phase Epitaxial Regrowth (SPER) or laser annealing will be introduced as scaling progresses. To preserve the abruptness and low sheet resistance of the extension junctions, the thermal budget related to silicide formation has to be reduced as much as possible. Reducing the silicidation temperature makes the nucleation of the Co-disilicide more difficult resulting in increased silicide / silicon interface roughness. Reducing the silicidation temperature from 800ºC to 700ºC causes a significant increase of the reverse bias junction leakage (shown in Figure 3 for 70 nm deep As junction). It is studied whether alloying the Co with Ni can improve the junction leakage for reduced silicidation thermal budget. Ni-silicide, which can be obtained at temperatures below 500ºC, is an attractive alternative for Co-silicide. The trade-off between junction leakage and silicide sheet resistance is studied for Co-silicide, CoNi-silicide and Ni-silicide.

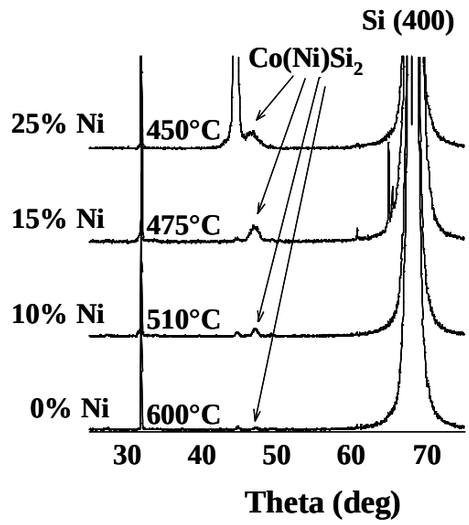

Figure 1 : Nucleation of Co-disilicide from CoNi alloy films with different Ni concentration.

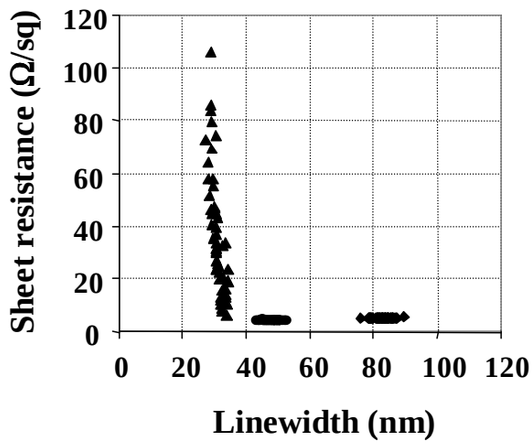

Figure 2 : Sheet resistance of Co-silicide As doped poly-gates versus gate length.

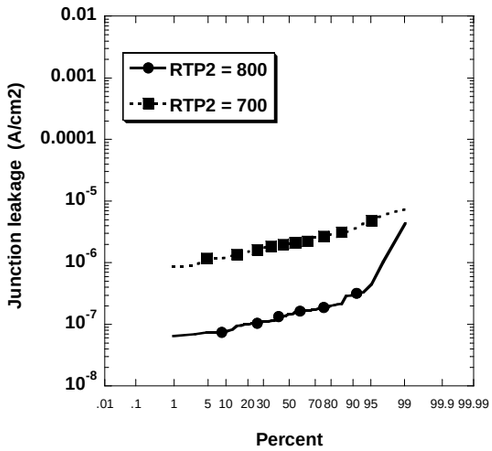

Figure 3 : Junction leakage of Co-silicided 70 nm deep As junctions for silicidation at 800 and 700ºC.