Ni Based Silicides: Material Issues for Advanced CMOS Applications

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For the 65 nm CMOS node and beyond, with gate lengths below 40 nm and junctions depths under 100 nm, self-aligned silicide (SALICIDE) processes face increasingly challenging constraints. With limitations for Co based silicides, particularly in meeting sheet resistance requirements on sub-40 nm gate lengths, attention has moved towards Ni based silicides.

This paper presents a study of key materials issues for Ni based silicides and their impact on CMOS applications. Fundamental aspects of the silicidation reaction are addressed, such as the reaction kinetics, mechanisms of thermal degradation, effect of alloying elements, capping layers, thickness scaling and effects of substrate crystallinity and dopants, as well as their implications for implementation into advanced CMOS flows.

In contrast with Co based silicides, Ni silicide can achieve low sheet resistance at gate lengths well below 40 nm (Fig. 1). In general, a reverse linewidth effect is observed both on gates as well as S/D areas, due to an increase in silicide thickness with decreasing feature dimensions. This effect, if excessive, can lead to issues such as yield degradation and increase in diode leakage. In order to develop an optimized RTP process, providing an optimal control of the silicidation reaction, the kinetics of Ni silicidation were studied under conditions suitable for applications into future CMOS nodes, including the effects of dopants, substrate crystallinity and pre-treatments (Fig. 2).

The effects of capping layers were also studied, as well as the effect of scaling the Ni thickness, finding limitations on thickness scalability.

Thermal stability is also a significant issue for NiSi. Degradation at moderate temperatures occurs either by transformation to the higher resistivity $NiSi_2$ phase or by changes in film morphology (agglomeration or inversion). Thermal degradation was studied as a function of film thickness. The effects of alloying elements such as Pt on thermal stability were studied as well (Fig. 3), for different substrate doping and crystallinity, under conditions suitable for advanced CMOS applications. Although the addition of Pt is expected to stabilize NiSi against transformation to $NiSi_2$, we show that it can also improve the stability of NiSi against morphological degradation.

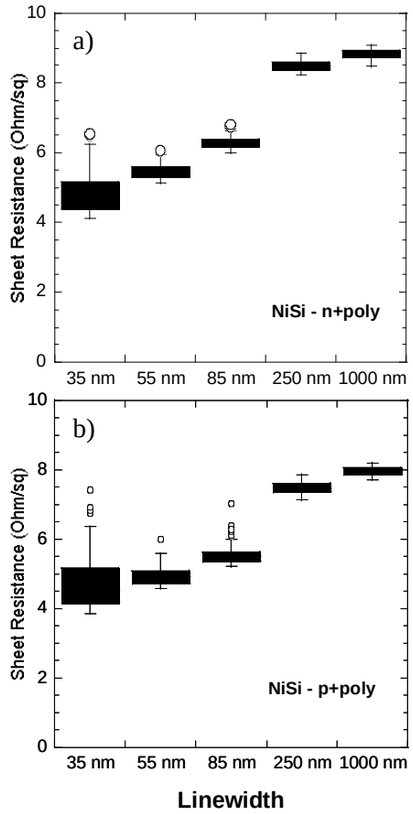

Fig. 1. Sheet resistance vs linewidth for NiSi on (a) n+ and (b) p+ poly Si gates. A reverse linewidth effect due to thickening of the silicide on narrower gates is observed.

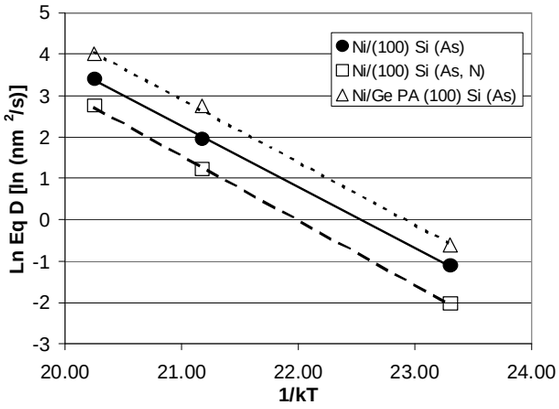

Fig. 2. Reaction kinetics for Ni on (100) As doped Si, showing the effects of N co-doping and of Ge pre-amorphization. Studies were performed on As and on B doped (100) Si and poly Si samples.

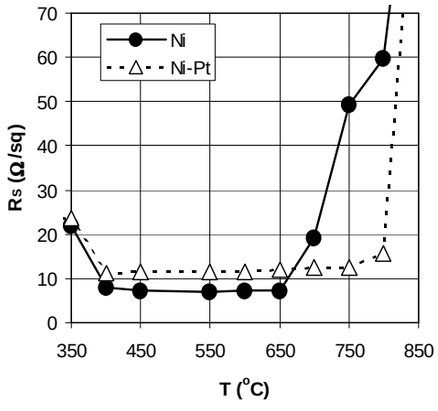

Fig. 3. Sheet resistance as a function of temperature for Ni and for Ni-Pt silicides on As doped (100) Si.