## CHARACTERIZATION OF HIGH-K Hf-SILICATE GATE DIELECTRIC FILM SYSTEMS PROCESSED BY RTA, SPIKE AND FLASH ANNEAL

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The 2001 edition of the International Technology Roadmap for Semiconductors (ITRS)<sup>1</sup> specifies a source/drain extension junction depth of less than 17nm and sheet resistance less than 760  $\Omega$ / for the 65nm technology node. The increased stringency of the depth requirement is not fully ameliorated by the relaxation of the sheet resistance. Recently, dopant diffusion using advanced annealing technologies such as spike and Flash anneals have been studied extensively<sup>2</sup>. These annealing techniques reduce junction depth and increase activation by optimizing the thermal budget. In this study, it is shown that approximately 10nm can be gained for a Flash anneal (fRTP) over an Impulse anneal (iRTP), with similar dopant activation, for p and n-type low energy implants, as shown in Figure 1. Integration of aggressive annealing technology with high-k materials is of increasing concern as the two technologies come closer to viability and necessity.

As complimentary metal oxide semiconductor (CMOS) devices continue to scale with the rapid performance pace of Moore's Law, gate dielectric materials with significantly higher dielectric constants (k = 10 - 25) are being investigated as potential replacements for silicon dioxide,  $SiO_2$  (k = 3.9), and silicon oxynitride, providing opportunities for introduction of a physically thicker film, with lower leakage current and with capacitance equivalent to < 1.0nm SiO<sub>2</sub>.<sup>3-5</sup> Changes in the composition of candidate materials; metal-organic chemical vapor deposited (MOCVD) hafnium silicate (40nm) (Hf<sub>x</sub>Si<sub>1-x</sub>O<sub>2</sub>  $(0.8 \ge x \ge 0.4)$  has been evaluated by several techniques including; X-ray diffraction (XRD), X-ray reflectivity (XRR), scanning electron microscopy (SEM), high resolution transmission electron microscopy(HRTEM) and high angle annular dark field scanning transmission electron microscopy with electron energy loss spectroscopy (HAADF-STEM-EELS). Phase segregation and crystallization during fRTP and iRTP anneal have been observed and compared with those observed for traditional rapid thermal anneal (RTA). Trends were progressive with both metal content and the thermal budget of the anneal. Figure 2 shows the trend phase segration with metal composition for an impulse anneal to 1050C. Since these physical characteristics influence the electrical performance of high-k capacitors and transistors, understanding the mechanisms associated with leakage current remains a primary challenge.

## REFERENCES

<sup>1</sup> International Technology Roadmap for Semiconductors - Front End Processes, Semiconductor Industry

Association, p. 20, 2001 <sup>2</sup>D.Camm, et. al., "Engineering Ultra-Shallow Junctions using fRTP" in RTP Conference 2002.

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Figure 1. SIMS profiles of BF<sub>2</sub> (2.2keV, 1E15) implants annealed by fRTP and iRTP. Activation levels are similar for the two profiles shown.





Figure 2. HAADF-STEM images of Hf-Silicate films after iRTP anneal with peak temperatures of 1050C.