Fabrication of SiGe-on-insulator substrates for high-performance strained SOI-MOSFETs by Ge-condensation technique

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A strained SOI-MOSFET is a promising device concept for high-performance CMOS applications, since the device can enjoy all the merits of strained Si channel and the SOI structure [1]. In order to give a tensile strain to the channel, the strained Si channel layer is pseudomorphically grown on a lattice relaxed SiGe-on-insulator (SGOI) substrate, having a larger lattice constant than that of Si. SGOI substrates have been fabricated so far by the SIMOX [2] and wafer bonding techniques [3]. However, the Ge fraction is essentially limited only to 15% for the former [4], and the threading dislocation density is as high as $10^5 cm^{-2}$ for the latter [5]. Recently, we have developed a novel fabrication method for SGOI substrates, the Ge-condensation technique [6], in order to overcome the above significant problems. A variety of SGOI structures have been fabricated by this method for FD- and PD-strained-SOI MOSFETs and even for SGOI-MOSFETs with strained SiGe channels [7]. In this paper, the Ge-condensation technique is reviewed and recent experimental results are presented.

The fabrication procedure of a SGOI substrate and a strained Si layer is illustrated in Fig. 1(a)-(e). First, a pseudomorphic SiGe layer with low Ge fraction, x_i, is epitaxially grown on a conventional SOI substrate. The wafer is oxidized in O_2 atmosphere at a high temperature (>1000°C). During the oxidation, Ge atoms are rejected from the oxide layer into the remaining SiGe layer, and the interface between the Si and SiGe layers is diminished by the interdiffusion of Si and Ge atoms. The lattice relaxation also precedes via a slip at the SiGe/oxide interfaces. This process results in pure SiO_2 layer and SiGe layer of the final Ge fraction x_f of $x_i(T_i/T_f)$, where T_i and T_f indicates initial and final SiGe thicknesses. After the surface oxide layer is removed, a Si layer is epitaxially grown on the SGOI layer. The advantages of this method are listed as follows; (1) easy fabrication of ultra-thin SGOI layer with high Ge fraction, (2) low threading dislocation density ($<1000 cm^{-2}$), (3) good surface morphology (*rms*<0.45nm) without CMP, (4) simple procedure which can be easily merged into CMOS processes.

An example of the fabricated ultra-thin strained SOI substrate with the body thickness of 21 nm is shown in Fig. 2. The strained Si layer with 1% of tensile strain was formed on the SGOI layer of 50% relaxation. According to systematic experiments, it was found that larger T_i and/or mesa isolation prior to the oxidation is effective for enhancing the relaxation of the SGOI layers [8]. The latter method drastically improved the *rms* of the surface roughness down to 0.17nm.

Strained-SOI MOSFETs with the SGOI substrate of thicker and higher relaxation ratio were fabricated by the Ge-condensation technique [9]. The drain current for the long channel nMOSFET was increased by 70% than that of the control Si nMOSFET due to the electron mobility enhancement (Fig. 3). On the other hand, it was found that the mobilities were degraded for thinner strained Si layers due to the Ge diffusion from the SGOI layers to the gate oxide interfaces. The scaling down of FD strained SOI-MOSFETs inevitably demands ultra-thin strained Si layers. Therefore, the Ge diffusion out of the SGOI layers should be carefully controlled by introducing rapid or low temperature activation processes.

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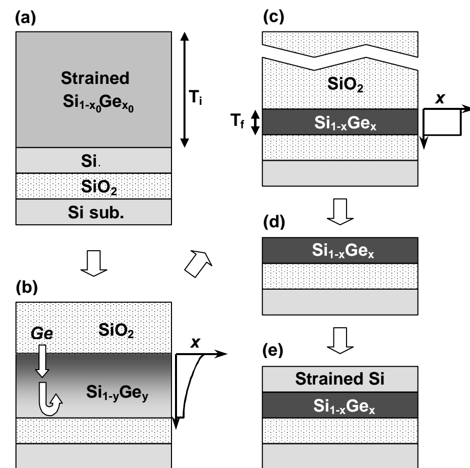

Fig. 1 Fabrication procedure of a SGOI substrate and a strained Si layer on it by the Ge-condensation technique.

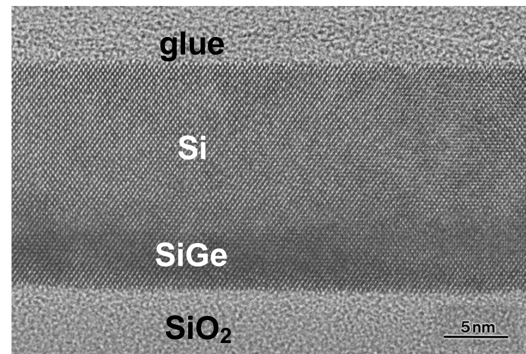

Fig. 2 Cross sectional TEM image of an ultra-thin strained Si layer on a SGOI substrate

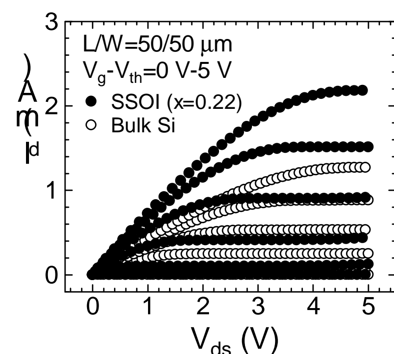

Fig. 3 Comparison of drain current of the strained SOI-nMOSFET and the control Si-nMOSFET.