

MOSFET Channel Engineering using Strained Si, SiGe, and Ge Channels

E.A. Fitzgerald, M.L. Lee, C.W. Leitz, D.A. Antoniadis¹
 MIT, Department of Materials Science and Engineering,
¹Department of EECS, Cambridge, MA 02139, USA
 Phone: +1-617-258-7461 Fax: +1-617-253-3046 Email:
efitz@mit.edu

1. Introduction

Epitaxial relaxed SiGe buffer layers [1] create a larger lattice constant on a Si substrate, allowing subsequent SiGe layers to be strained in tension or compression. Early work in application of strain via relaxed SiGe concentrated on investigating elevated carrier mobility in pure tensile Si layers deposited on relaxed Si_{1-x}Ge_x. [2][3]. Relatively short channel MOSFETs containing strained Si have shown that higher mobility and drain current measured in long channel devices are retained at shorter channel lengths. [4][5] A quantitative method to correlate the effect of mobility enhancement in long and short channels shows that approximately 50% of the long channel drain current enhancement is obtained in shorter channels. [6] Thus, large MOSFET devices can be used to rapidly probe heterostructures for channel enhancement, as well as limits to processing. [7][8] In this summary, we report on probing advanced SiGe heterostructures to understand the potential of strained Si/SiGe heterostructures in MOSFETs.

2. Single Strained Si Channels on Relaxed Si_{1-x}Ge_x

Tensile strain in Si increases the mobility of electrons nearly 80% over that in conventional MOS channels. [4][7] Holes also have increased mobility in strained Si; however, greater strain levels in the strained Si are required to achieve the same hole mobility enhancement as achieved for electrons. Also, hole mobility enhancement does not saturate as readily as the electron case. Fig. 1 shows the carrier mobility enhancement factors for electrons and holes as a function of Ge concentration in the relaxed Si_{1-x}Ge_x. The data are extracted from one-mask-step large gate length MOSFETs that have vertical electric fields in the channel comparable to MOSFETs with shorter gate lengths. The data for $x < 0.5$ are from references [7][8].

We report that significant mobility enhancement (enhancement factor 2.5) in PMOS devices can continue to increase in single strained Si layers with $x > 0.5$. Planar strained Si layers (partially relaxed through the introduction of dislocations) have been achieved on all buffer layer compositions, including pure Ge by very low temperature chemical vapor deposition ($T \leq 400\text{C}$).

3. Dual Channel Heterostructures on Relaxed Si_{1-x}Ge_x

Although hole mobility enhancements of 2.5 are even larger than the maximum electron mobility enhancement, we have shown that incorporating a compressively strained Si_{1-x}Ge_x layer below the tensile-strained surface Si layer increases the hole mobility to an even greater extent, without impacting electron enhancements. [9] Such dual channel heterostructures have shown hole mobility enhancement factors in *p*-MOSFETs as high as 8 at vertical fields of 0.65 MV/cm (with little sign of degradation as field is increased) for a structure of pure Si and pure Ge layers deposited on $x=0.7$. [10] We have also obtained high hole and electron mobility enhancements in a dual channel composed of pure Si and pure Ge on a 50% Ge substrate composition. Fig. 1 summarizes the best carrier mobility enhancements in large research

MOSFETs achieved to date for different heterostructures on relaxed Si_{1-x}Ge_x on Si.

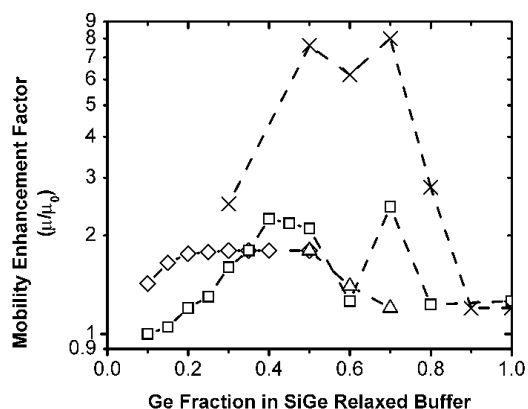


Fig. 1 Summary of mobility enhancements extracted from one-mask-level, large MOSFETs with a vertical effective field of approximately 0.6 MV/cm: single channel NMOS (diamonds), single channel PMOS (squares), dual channel NMOS (triangles), dual channel PMOS (crosses).

4. Digital Alloy Channels

Combining the single channel and dual channel data, we speculate that the heterostructures in many of the PMOS devices have a thickness less than the vertical extent of the hole wavefunction and therefore the properties of the hole is determined by a combination of the hole wavefunction in the gate dielectric, the strained Si, the compressed Si_{1-x}Ge_x (if present), and the relaxed Si_{1-x}Ge_x alloy. Layer thickness and vertical electric field are variables in determining the character of the hole wavefunction in the channel. To further elucidate this observation, we have built a digital alloy channel (greater than 100Å in total channel thickness) composed of extremely thin layers of tensile Si and Si_{0.3}Ge_{0.7} on a relaxed Si_{0.3}Ge_{0.7} substrate. The *p*-MOSFETs fabricated from this material show that the mobility enhancement factor (2.1) is independent of vertical field, as expected since the wavefunction is averaging over all of the digital alloy layers at all electric field values.

Acknowledgements

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