New Metal Gate Architecture Achieved by Chemical Vapor Deposition for a Complete Tunnel Fill

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As the standard CMOS is scaling down, the use of metal gate is known to solve the problems inherent to the poly-silicon such as high gate resistance, poly depletion or boron penetration into the channel. This metal gate can be realized by etching, by the damascene replacement technique (1) or by a total salicidation of a poly-silicon gate (2). However all those techniques have difficult drawbacks to manage.

This paper deals with a new method to realize such metal gate structure. A sacrificial conductor gate is deposited first in order to do the junction engineering in a conventional way. When the device is complete, middle end oxide is deposited and contacts are opened. Contacts on gate are used to isotropically etch the sacrificial gate by using SF_6 chemistry. The resultant is a tunnel gate that must be filled by the appropriate material. We have chosen to use a chemical vapor deposition of TiN using $TiCl_4$ and NH_3 precursors at a temperature of 630°C. This deposition technique has proven to be able to fill a tunnel of at least 2µm length with 100% step coverage (figure 1). The TiN / thermal oxide interface is smooth as visible from the high resolution TEM (figure 2). Hence at the same time contact and gate tunnel are filled then the metallic material must be removed on top by a CMP step. This tunnel gate has been successfully integrated into a 0.13µm process (figure 3).

Using this new integration scheme has the advantage to avoid cross-contamination problems by depositing metallic material once the contact is done. This metal gate structure is simple to achieve and the co-integration with poly-silicon transistor is feasible. Furthermore, other metallic material or deposition technique can be chosen in order to obtain the desired work function or to decrease contact and gate resistance. For instance we have also evaluated the TiN/W stack

This new integration scheme is a promising solution in the field of new devices such as a gate all around or double gate architecture.

REFERENCES

(1): K Matsuo, and al, VLSI Tech. Dig., 2000, pp70-71
(2) : B Tavel, and al, IEDM Tech. Dig., 2001, pp825-828

FIGURES

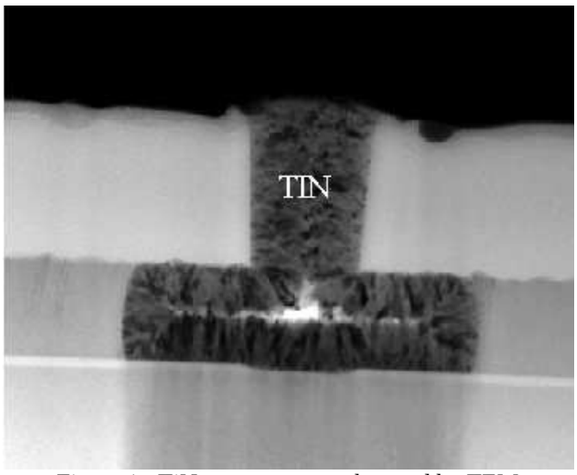

Figure 1 : TiN step coverage observed by TEM

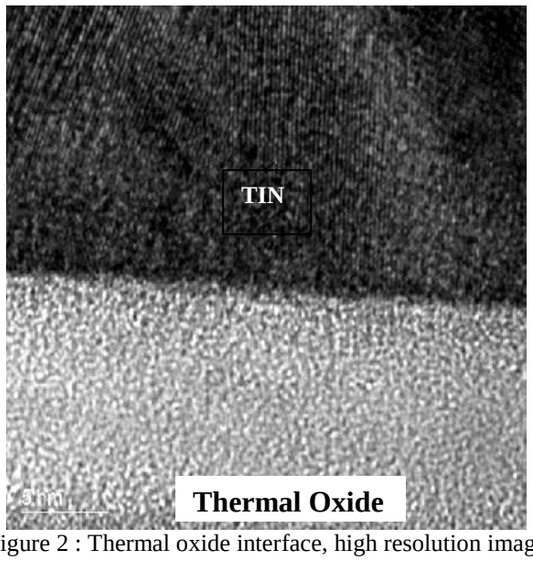

Figure 2 : Thermal oxide interface, high resolution image

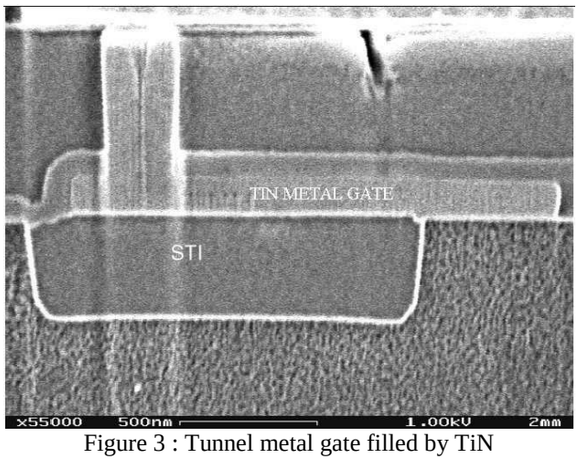

Figure 3 : Tunnel metal gate filled by TiN