Electron Trapping in the Conventional and Modified HfO_2 ALD Gate Dielectrics

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HfO_2 films deposited by the atomic layer deposition (ALD) method have been extensively studied as promising candidates for gate dielectric due to their high dielectric constant and good compatibility with the conventional poly-Si gate process [1]. However, the step-wise nature of the ALD coverage may result in variations of the local film density (voids) that limit film thickness scaling and may cause high gate leakage. In order to alleviate these process constraints, a modified HfO_2 ALD sequence, which significantly improved the film's electrical quality, was recently developed [2]. In the present work, we investigated the electrical properties and origin of charges in both the conventional and modified ALD HfO_2 gate dielectrics in connection with the specifics of the deposition process. Analysis of the electrical data suggests that ALD films contain both fixed bulk positive charges and electron traps, some of which are related to post ALD processing.

Wafers were processed with a standard N- and P-MOS process up to the gate dielectric deposition step. A nominal 3.0 nm HfO_2 layer was deposited using both the conventional and modified ALD sequences on an O_3 treated Si substrate, followed by a 600°C N_2 anneal and poly-Si gate electrode deposition; the process was then continued on a standard flow. The threshold voltage (V_t) of the NMOS transistors with conventional and modified ALD gate dielectrics shows similar reverse short channel effect (SCE), Fig.1. This may be attributed to the diffusion of the electron trap induced species from the gate perimeter that may occur during poly etch, subsequent ash/clean and spacer deposition. To verify this assumption, a seal nitride (SN) layer was introduced into the process flow after the poly definition and clean step. The SN eliminated the reverse V_t roll off and reduced V_t for the conventional ALD samples but the modified ALD gate dielectric retains the reverse SCE, though the V_t values were also reduced, Fig.1. This indicates that SN blocks the penetration of those trap-related species which are highly diffusive in the HfO_2 film (presumably from the spacer TEOS deposition process step) while the species with lower diffusivity (associated with poly etch and ash process steps) may still contribute to the reverse SCE in the case of the modified ALD film due to the peculiarities of the film structure.

A characteristic feature of the modified ALD film (compared to the standard ALD) is that higher V_t values of the transistors fabricated with the modified ALD sequence are accompanied by higher transconductance values, Fig. 2, while the flat band voltage for both ALD processes is the same, Fig. 3. The proposed explanation invokes the presence of electron traps attributed to the modified ALD stack, their charging/discharging manifesting itself in higher threshold voltage and artificially higher peak mobility associated with the specifics of the transistor inversion layer formation.

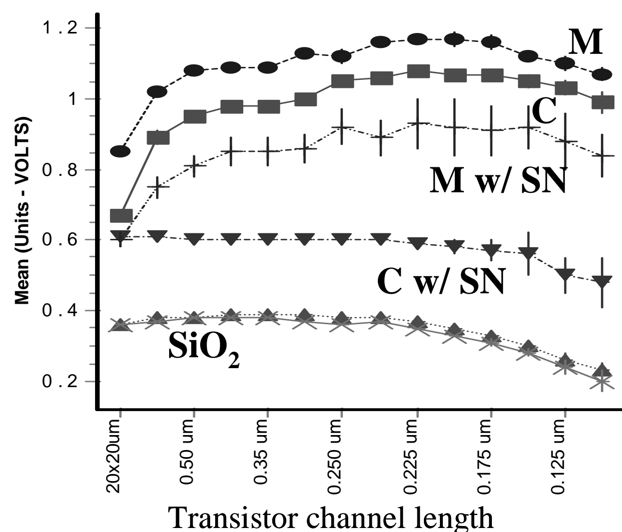

Fig. 1 Threshold voltage vs. drawn transistor channel length for conventional (C) and modified (M) HfO_2 ALD gate dielectric with (w/ SN) and without seal nitride layer. SiO_2 control data is included for comparison. Each symbol represents an average for the data from 2 wafers, 17 sites/wafer; the error bar is ±1 standard deviation.

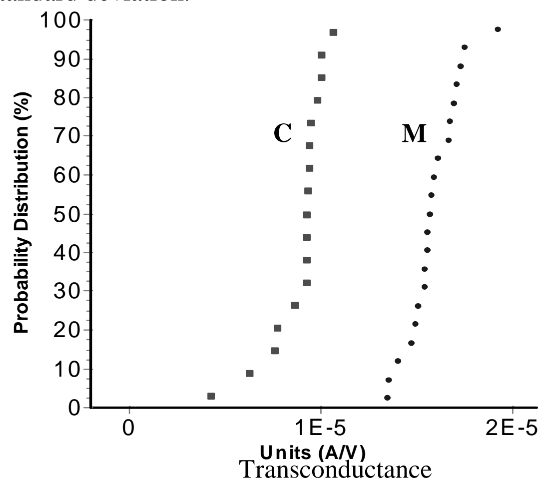

Fig. 2 Transconductance values of 20x20 µm transistors with conventional (C) and modified (M) HfO_2 ALD gate stack.

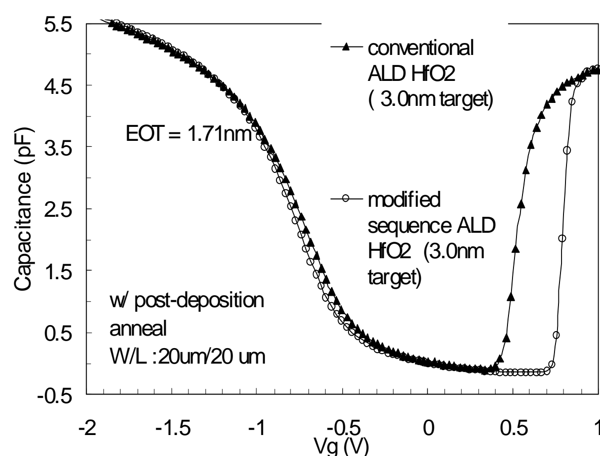

Fig. 3 Conventional and modified HfO_2 ALD gate stack CV data.

References

1.Y. Kim et al., IEDM Tech Digest, 455 (2001)
2. C. Lim et al., 2002 ECS Meeting, Salt Lake City, 2002.