CHARACTERIZATION OF MIST DEPOSITED $HfSiO_4/SiO_x/Si$ STRUCTURES

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The effect of an interfacial SiO_x in high-k dielectric MOS gate stacks is beneficial on one hand (superior electron mobility in the channel) and detrimental on the other (reduction of the capacitance of MOS gate stack). Consequently, understanding of the effects controlling formation and properties of ultra-thin interfacial SiO_x in high-k MOS gate structures is an important factor in the process of introducing high-k gate dielectrics into mainstream Si manufacturing.

The goal of this experiment was to characterize $HfSiO_4/SiO_x/Si$ MOS gate structures in which the high-k layer was formed by mist deposition and an interfacial SiO_x film was grown in the course of post-deposition RT treatments of the Si wafer. The focus of this investigation was on the interactions of Hf from mist deposited $HfSiO_4$ with the underlying SiO_x. In this work ultra-thin (<5 nm) films of $HfSiO_4$ were mist deposited [1] from a liquid source on oxide-free (HF-last process) or UV/NO treated [2] Si surfaces. During subsequent thermal curing (150 ^oC and 260 ^oC) and annealing steps (spike anneals at 600 ^oC) in N_2 an interfacial oxide was formed on the Si surface. As determined by TEM, regardless of the thickness of the $HfSiO_4$ film, thickness of this oxide was consistently in the range of 2.2-2.6 nm (Fig. 1) depending on the pre-deposition surface treatments. However, electrical characterization of $Pt/HfSiO_4/SiO_x/Si$ devices (Fig.2) has shown EOT in the range of 1.4 nm for these structures indicating some penetration of Hf into the interfacial oxide. XPS characterization of interfacial SiO_x, combined with selective etch back of $HfSiO_4$ films, did shown up to 3 at.% Hf penetration of the uppermost part of the interfacial oxide. Considering structural stability of mist deposited $HfSiO_4$ during RT anneals carried out in addition to post-deposition thermal sequences (up to 20 sec. long anneal at 1000 ^oC does not seem to affect structure of the film as shown by XRD results in Fig.3) it is assumed that more Hf can be incorporated in the interfacial oxide in the case post-deposition spike anneals are carried out at temperatures higher than 600 ^oC. Then, taking advantage of the high etch selectivity of mist deposited $HfSiO_4$ to underlying interfacial SiO_x the upper layer can be etched off leaving a Hf-rich ultra-thin thermal SiO_x layer to act as a gate oxide. Relevant experimental results are presented in the full account of this work.

[1] D.-O. Lee, P. Roman, C.-T. Wu, P. Mumbauer, M. Brubaker, R. Grant, and J. Ruzyllo, *Solid-State Electronics* (in print).
[2] P. Roman, D-O. Lee, J. Wang, C-T. Wu, V. Subramanian, M. Brubaker, P .Mumbauer, R. Grant and J. Ruzyllo, *Proc. Seventh Intern. Symp. on Cleaning Technol. in Semicon. Dev. Manufacturing*, Eds. J. Ruzyllo, T. Hattori, R. Opila, and R. Novak, Electrochem Soc. Proc. Vol. PV 2001-26, 2002, 241-248.

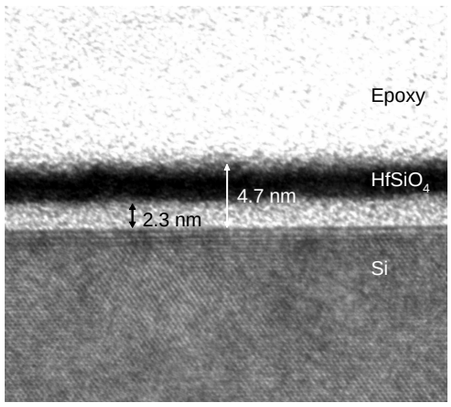

Fig.1 ***TEM cross-sectional view of 4.7 nm thick $HfSiO_4$ deposited on UV/NO-last Si surface.***

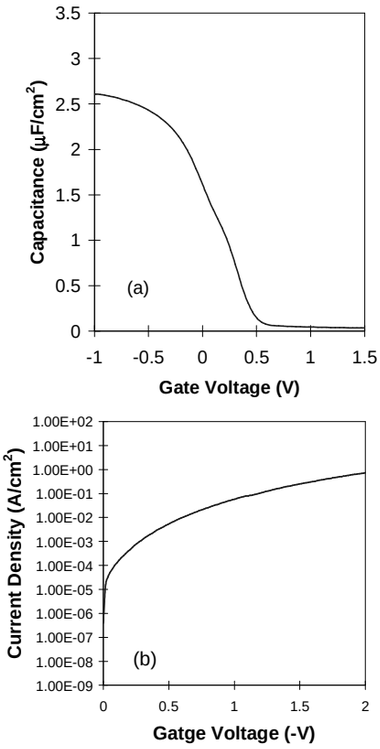

Fig. 2 Example of (a) C-V (b) J-V characteristics of 4.7 nm thick mist-deposited $HfSiO_4$.

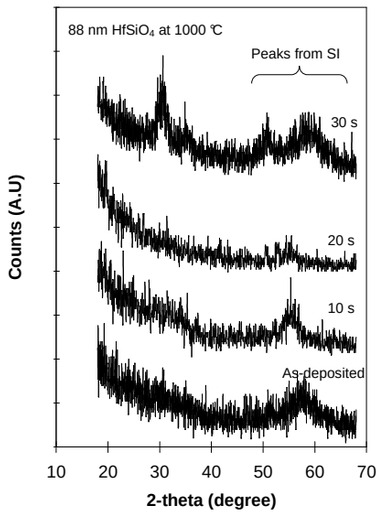

Fig.3 XRD pattern of 88 nm thick $HfSiO_4$ annealed in a RTP chamber at 1000 °C in N_2 at different times.