

## DRAM TECHNOLOGY FOR 100NM AND BEYOND

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The key challenges for scaling of DRAM cells are reviewed for „trench capacitor cells“ and „stacked capacitor cells“. Both cell types have to implement significant innovations for 100nm and beyond (Fig. 1, 2). Cell layout/design has to be innovated for both cell types. New materials have to be introduced like hi-K materials for capacitor, W/WN gates for gate resistance reduction, low-K materials for reduced parasitic capacitance. Transistor construction is another key element in scaling. Patterning, especially lithographic techniques, have to be significantly improved. This paper gives an overview on the DRAM roadmap for both cell technologies; especially the viability of trench technology down to 70nm is demonstrated.

For the evolution of trench capacitor technology (Fig. 1, 2, 3) towards 70nm capacitor enhancement techniques are important. Here several options are shown (see also 1):

- HSG in trench provides a capacitance enhancement factor up to 50 %, depending on the grain size of HSG-poly (Fig. 4)
- Trench bottling: While the trench diameter in the upper 2µm of the trench is kept at the level required by cell groundrules, the lower part of the trench can be widened. A capacitance enhancement of around 30 % has been shown for 110 nm groundrule..
- Dielectric: The conventional NO dielectric can be replaced by a hi-K material, which is compatible with trench technology, e.g. Al<sub>2</sub>O<sub>3</sub>.
- Combinations of all 3 options can be chosen to secure the trench capacitance roadmap down to 70 nm groundrules.

Besides trench capacitance the reduction of leakage currents is key for DRAM technology, with focus on the subthreshold current of the cell transistor and the junction leakage from the storage node to the substrate.

For a planar trench transistor cell and also for stacked capacitor cell the separate optimisation of doping profiles at both sides of the transistor is of similar importance. The electric field at the storage node has to be reduced. Key options for optimisation of doping profiles are discussed (see also 3).

Also the option of a vertical trench cell (4) –which does not need to scale down the transistor length of the cell device as aggressively as planar cells is - discussed and compared to planar cells.

DRAM technology at 100nm and beyond will also have important innovations in e.g. gate material: to reduce the resistance of the gate electrode/wordline W/WN gate

stacks will be the common feature of DRAMs below 100 nm.. A resistance of less than 6 Ohm/sq can be achieved with only half the thickness compared to WSi gate stack.

For scaling of DRAM cells lithography is a key enabler. 193 nm ArF lithography is a must below 100 nm resolution. It has to be combined with resolution enhancement techniques.

„Strong“ enhancement techniques like double exposure techniques such as dipole illumination or alternating Phase Shift Masks (conventional and chromeless) will become more important on the way towards 70nm.

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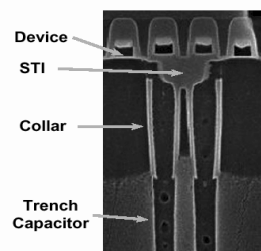


Fig. 1: Trench DRAM cell (planar)

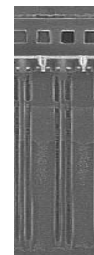


Fig. 2: 110 nm Trench DRAM cell

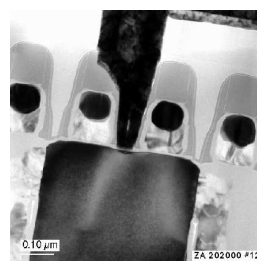


Fig. 3: TEM of 110 nm DRAM cell



Fig. 4: Trench capacitor with HSG surface enhancement (1)