FeRAM Technology : Today and Future

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Introduction

Ferroelectric random access memory (FeRAM) has been intensively studied because of its superior performance as a non-volatile memory. Lower power consumption, faster read/write cycle and longer endurance compared to a conventional EEPROM are suitable for various non-volatile applications. In addition, the memory cell structure similar to dynamic random access memory (DRAM) indicates a high potential to realize large scale FeRAM with 1G-bit or higher density. FeRAM process technology is basically compatible with that of logic devices. This feature enables FeRAM to extend the application area from pure memory to embedded memory. Although FeRAM is recognized as a universal memory because of such superiority, further innovations are needed to realize the replacement of all memories to FeRAM. In this paper, a new FeRAM structure called Chain-FeRAM™ [1] is presented which satisfies both a faster operation and a small chip size. In addition, a new electrode technology using SrRuO3 stack [2] is discussed which realized superior write/read endurance and was successfully implemented to a recently developed 1T1C 8Mb Chain-FeRAM™ . This electrode technology is a promising candidate to realize the replacement of high-end SRAM and DRAM which require the endurance up to 10^{15} cycles to FeRAM. Further more, the other important technologies that dominate the future scalability of FeRAM will be discussed.

Chain-FeRAM™ structure

Figure 1 shows a schematic drawing of the 8Mb Chain-FeRAM™ structure. The unit cell was formed by one transistor and one ferroelectric capacitor which were connected in parallel. 8 unit cells were connected in each cell block. A block select transistor exists in one side of the cell block, and a plate line was connected to another side. During the operation, one capacitor was selected randomly by cutting off its pare transistor. By using this architecture, the number of plate line driver circuit was reduced to 1/8 compared to a conventional type architecture. As the result, the cell efficiency in a chip increased up to 60%. At the same time, due to the lighter bit-line capacitance, it realized faster device operation.

Both sides SRO electrode technology

Both-sides thin $SrRuO_3$ (SRO) (BSTS) electrode technology has been successfully developed to realize highly reliable sub-micron $PbZr_xTi_{1-x}O_3$ (PZT) capacitor. It was found that 10nm-thick SRO films on the both sides of PZT film dramatically improved the electrical performance of capacitor such as switching charge (Qsw), saturation characteristics of hysteresis curve and fatigue endurance compared to the conventional capacitor without SRO. Figure 2 shows the comparison of hysteresis curves of PZT cell capacitor array for (a) conventional Pt electrodes without SRO, (b) Bottom-SRO without Top-SRO, (c) Top-SRO without Bottom-SRO and (d) BSTS. It was found that the hysteresis shape was highly improved from (a) to (d) and the BSTS sample showed the best rectangular shape which indicated a good saturation characteristics. This technology was successfully implemented to 8Mb-FeRAM that showed a wide signal margin for 1T1C operation. Figure 3 shows the cross sectional view of the 8Mb-FeRAM 'Chain'-cell.

Summary

In this paper, break through technologies for future high density FeRAM including cell architecture and electrode material were presented. In addition, the other key process technologies which realize high reliability and smaller cell dimension will be discussed with a forecast of future FeRAM.

References

[1]D.Takashima et.al., ISSCC, 787-792,May 1998
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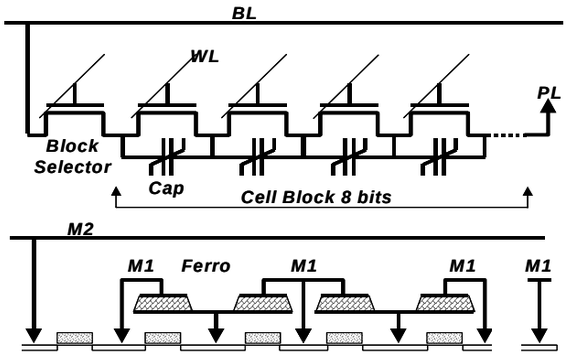

Fig. 1 Chain-FeRAM architecture

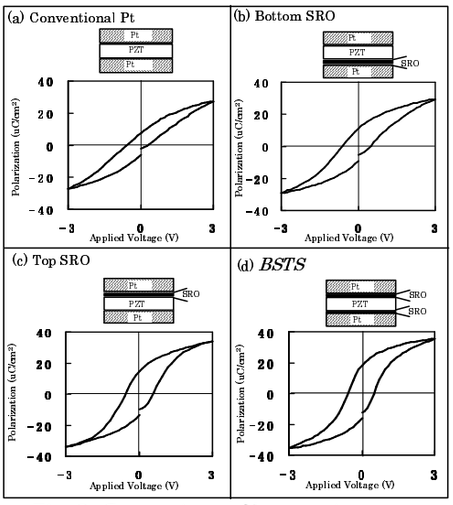

Fig. 2. Comparison of hysteresis curves

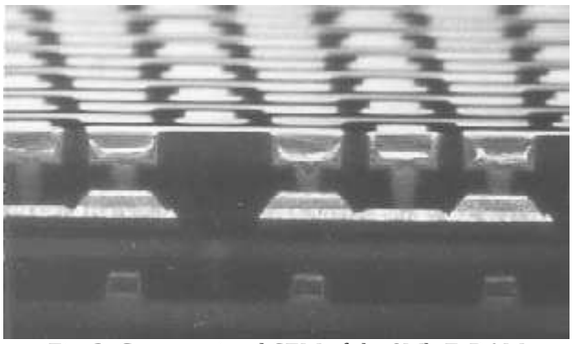

Fig. 3. Cross sectional SEM of the 8Mb-FeRAM