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A Novel Approach to Contact Integration at 90-nm and Beyond

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Abstract

A contact integration, with low defect density, for 90-nm CMOS technology node is demonstrated. Patterning was achieved using 193nm lithography with a novel approach. Unique etch processes were developed to achieve sub-100nm contact CD and vertical sidewall. Defect improvement for this novel integration is presented. Improvements in electrical leakage performance are presented for this integration. Measurements of contact-to-poly-Si gate capacitance reveal dramatic reduction with shrunk contact CD achieved in this integration.

Introduction

Contact module must continue to be scaled with shrinking technology. This has proven difficult, as others have used complex integration methods to scale the contact CD down [1]. We reported a SRAM cell size of $1.33\mu m^2$ for the 90-nm technology node, and use of novel 193nm-patterning methods at critical layers such as contact (CD target of 120nm), gate, and active [2]. The difficulties of feature shrinkage, e.g. to achieve smaller bitcell size, at 90-nm technology node and below arise from challenges in lithography, e.g. through-pitch CD uniformity, and a common depth of focus [3, 4]. These challenges are shared by etch processes, targeting contact holes with a desired geometry i.e. CD and taper. Small contact CD not only benefits leakage behavior, e.g. contact-to-gate, etc. but it will also improve contact-to-gate capacitance. However, defect density rises as contact size is shrunk. Therefore, a contact integration scheme capable of producing small contacts, but with low defect density is necessary. Here, we report such a contact integration which can achieve contact CD's less than 100nm.

Experiments

New patterning processes using 193nm lithography were developed and implemented to print contact holes. The use of a novel approach combining the lithography and etch, enabled us to gain dramatic etch CD biases to improve lithographic margins. Strong off-axis illumination was used in combination with a unique, aggressive model-based OPC scheme to allow robust contact-hole patterning through pitch with lower cost binary reticles. Etch processes were developed, to optimize the post-etch-contact geometry. In-line defect-density was measured on the 4Mb SRAM array using voltage contrast microscopy. Electrical leakage currents (contact-to-poly, contact-to-M1, and contact-to-active) and contact-to-poly-Si gate capacitance were measured. Cross-section, planar SEM inspections of these devices including contacts were carried out.

Results and Discussion

Fig.1 is an example process margin analysis for contact-to-metal1, where the metal1-to-metal1 space is 120nm [2]. With an assumed minimum isolation distance of 30-60nm, an overlay error ranging between 20-30nm, a metal1 and contact CD variation of between 5-15nm each, a contact top CD of 120-240nm can be derived. Contact top CD of <125nm was achieved using a combination of novel 193nm lithography and etch processes including fluorinated gas mixtures (Fig.2). We note that contact side-wall-angle improved ~13% (more vertical), while progressing from "Initial Etch" to "Improved Etch". Further, the contact-top CD was reduced by ~30% from "Initial Etch" to "Improved Etch". Contact-to-poly, to-ACTIVE, and to-M1 leakage measurements reveal superiority of the "Improved Etch" over "Initial Etch" (Figs. 3-5). This superiority, even at sub-nominal isolation, arises from smaller top CD, and steeper side-wall-angle achieved with this integration. Contact CMP was optimized to ensure excellent contact-to-M1 leakage (Fig. 5). Fig. 6 is a SEM x-section image of a contact with final CD of <90nm at the bottom and <110nm at the top achieved with the above integration.

Table I shows representative contact Kelvin resistance data for technology nodes down to 90nm. Due to area scaling and increasing dominance of glue/barrier/tungsten interfaces, we note a nearly 2x increase from 130nm technology node. Fig. 7 shows in-line defect-density measured as a function of ADI (after-develop-inspection) CD on 4Mb SRAM array such as shown in Fig. 8. The figure reveals a dramatic improvement with ADI CD x+10nm and above. It may be concluded that a usable exposure and defect density exhibit a competing behavior. Fig. 8 illustrates top-down and x-section images revealing contact size reduction between the two etch processes, "Initial Etch" and "Improved Etch". We note that for equivalent poly-Si gate-width and overlay, isolation between contact and gate can be improved by reducing the contact CD. Fig. 9 compares contact-to-gate capacitance measurements for "Initial Etch" and "Improved Etch" as a function of drawn isolation (40 to 90nm) along the x-axis. We note that the relative capacitance (arbitrary units), for the "Improved Etch", which achieved contacts 30nm smaller, is 4% lower for PMOS and 7% for NMOS. Further, the plots show that the capacitance, for the contacts with smaller contact CD, is insensitive to the drawn isolation down to 40nm space. This capacitance benefit from "Improved Etch" with smaller CD can be advantageous in high performance circuits.

Conclusions

A contact-integration, capable of achieving sub-100nm contact size and contact-side-wall angle of ~86° has been demonstrated. Novel 193nm patterning methods, in combination with new etch processes enabled such aggressive contact geometries for 90nm technology node and beyond. In-line defect-density measurements reveal high sensitivity to light-intensity. A compromise between largest contact CD and electrical leakage is critical. With this integration, improvement was discovered, comparing contact-to-gate capacitance for reduced contact CD achieved. Excellent electrical leakage performance attests to the robustness of this integration and potential beyond the 90-nm technology node.

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