

## BiCMOS Integration of High-Speed SiGe:C HBTs

H. Rucker, B. Heinemann, R. Barth,  
D. Knoll, D. Schmidt, and W. Winkler

IHP

Im Technologiepark 25,  
15236 Frankfurt (Oder), Germany

We describe the integration of high-speed SiGe:C HBTs with ring oscillator delays of 4.2 ps and  $f_T/f_{max}$  values of 180/200 GHz in a 0.25  $\mu\text{m}$  CMOS platform. Simple BiCMOS integration is facilitated by an HBT module without deep trench isolation and with low-resistance collectors formed by high-dose ion implantation after shallow trench formation. Excellent manufacturability and high yield are demonstrated.

### Introduction

High speed SiGe BiCMOS technologies facilitate single chip solutions for broadband and wireless communication systems. A major challenge for BiCMOS integration is to combine the potential of SiGe HBTs for ultra high speed operation with low process complexity. (1,2)

Here, we demonstrate a novel construction for high-frequency NPN devices without deep trenches and with low-resistance collectors formed by a high-dose implant after shallow trench formation. The new high-speed HBT module was integrated in a 0.25  $\mu\text{m}$  CMOS platform, leaving CMOS device characteristics unchanged. Excellent static characteristics and high yield of 4k transistor arrays were achieved. CML ring oscillator delays of 4.2 ps are demonstrated for HBTs with  $f_T/f_{max}$  values of 180/200 GHz.

### Device Design and Fabrication

The key new device features are the formation of the whole HBT structure in one active area without shallow trench isolation between emitter and collector contact (Fig. 1). This allows us to achieve collector resistances, which are even lower than the emitter resistance, and to reduce device dimensions and parasitic capacitances.

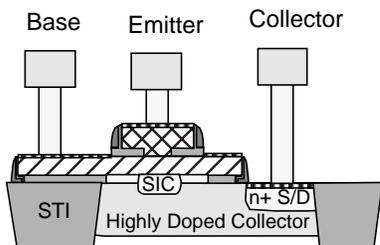


Fig. 1. Cross-section of the new HBT structure.

The flow of the BiCMOS process starts with the formation of the shallow trench isolation (STI), the CMOS wells and gates. The HBT module is introduced after CMOS gate spacer etching. It begins with the deposition of a layer stack protecting the CMOS devices. A resist mask is used to remove the protection layer from HBT regions and to define the collector wells by high dose ion implantation. The collector wells are confined by the STI side walls. Next, an oxide layer is deposited and structured to define the active collector region. A Si buffer layer, the SiGe:C base layer, and a Si cap layer are deposited in one epitaxial step. The following process flow of the HBT module is performed as in (2), involving 3 mask steps to structure the emitter window, the emitter poly, and the base poly. The fabrication is

completed with S/D implantation/anneal, a salicide blocking mask for poly resistors, cobalt salicidation, and structuring of four metal layers with a MIM capacitor.

### Device Results

Compared to previously demonstrated concepts, the new collector design achieves lower collector resistances, smaller collector-substrate junction areas, precise tailoring of the base-collector width, and improved heat dissipation due to the absence of deep trenches. The sheet resistance of the collector wells is about 27  $\Omega/\text{sq}$ . Excellent static characteristics and high yield of 4k HBT arrays demonstrate the low defect densities of the heavily doped collector wells (Fig. 2).

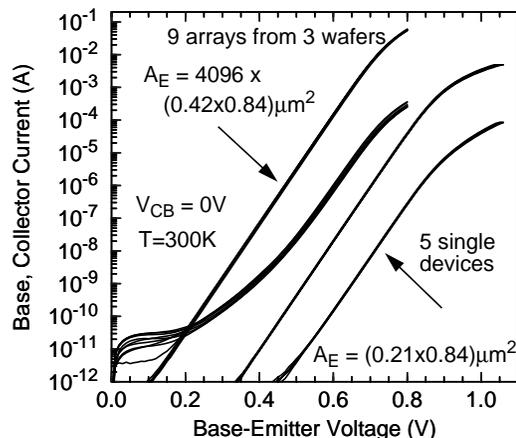


Fig. 2. Gummel plots of single devices and arrays at  $V_{CB}=0\text{V}$ .

The base-collector depletion width was optimized for best RF performance by adjusting the buffer thicknesses of the epi layer. Transit frequencies  $f_T$  and maximum oscillation frequency  $f_{max}$  vs. collector current for HBTs with drawn emitter areas  $A_E=0.21 \times 0.84 \text{mm}^2$  are shown in Fig. 3. The digital circuit performance was benchmarked using CML ring oscillators with 53 stages. The achieved gate delay of 4.2ps approaches the best reported values (3) and has not been demonstrated for a BiCMOS process so far.

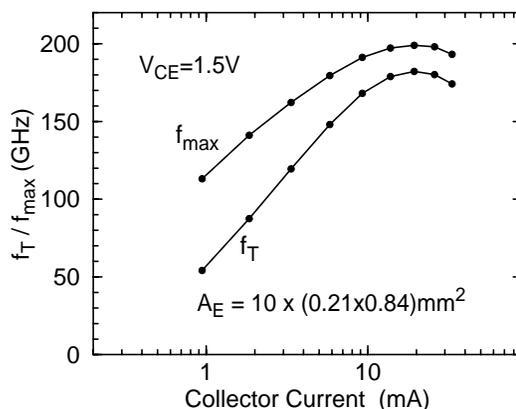


Fig. 3. Transit frequency  $f_T$  and maximum oscillation frequency  $f_{max}$  vs. collector current at  $V_{CE}=1.5\text{V}$ . Ten transistors in parallel were measured.

### References

- (1) D. Knoll et al., Proc. BCTM 2002, p. 162.
- (2) B. Heinemann et al., Techn. Digest IEDM 2002 (accepted paper)
- (3) B. Jagannathan et al., IEEE Electron. Device Lett. **23**, 541 (2002).