Differential Silicide Thickness for ULSI Scaling

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Abstract

We investigate the formation of $CoSi_2$ over a wide temperature range (275-450C for the first of a 2-step formation). The data fit nicely to a Deal-Grove[1] model. With appropriate times and temperatures, one can obtain significantly thicker silicides on poly than on mono Si (50-80%). This is useful for CMOS, allowing low resistance gates while minimizing silicide spiking in the junctions.

Experiment and Analysis

Recognizing that oxidation differs between polysilicon and monosilicon, and noting the work of d'Heurle[2], which indicates that grain boundaries can reduce reaction barriers for silicidation, we hypothesized that it may be possible to find an optimum temperature for silicidation to obtain the desired thickness differential. 200mm CZ silicon wafers, with or without an undoped poly (1500A thick on 30A SiO2), received HF dip and RF sputter preclean, depositions of 100A or 150A Co, with 150A TiN cap. These were reacted at 375-450C for times of 10-120s. Any unreacted Co was etched off, and all were given a final anneal of 700C/60s to transform from Co_2Si to $CoSi_2$. Sheet resistance (4-pt. Probe) and SEM X-sections provided estimates of the thickness of $CoSi_2$.

Figure 1 shows Conductivity vs. Sqrt(Time). Complete consumption of 100A Co corresponds to conductivity of 0.15 Ohm/Sq. In all cases below complete consumption of Co, poly samples gave greater conductivity, indicating thicker silicide growth. When the initial Co thickness is increased to 150A, the final $CoSi_2$ difference can increase to 60% (400C). These results prompted an additional study down to 275C, all with 150A initial Co. We then plot ratio of thickness on poly vs on mono silicon (Figure 2). Temperatures of 325-375C appear feasible, and can provide a significant difference in silicide thickness.

To study the thickness differences between mono and poly, we a)assume the final $CoSi_2$ thickness is 3x the thickness of the thickness after the first anneal, and b)apply a Deal-Grove model to this first anneal [Thk = (B*time)/Thk - A]. Figure 3 shows plots of Thk-vs-Time/Thk, from which we extract the parabolic and linear rate constants. In Figure 4, we see the parabolic rate constant (diffusion of species through the Co_2Si) has the same activation energy for both poly and monosilicon (2.4eV), indicating the $CoSi_2$ thickness differences are not due to differences in diffusivity through the Co_2Si. For t>>A^2/4B, a process is diffusion limited, while for t<<A^2/4B, it is reaction limited. Figure 5 plots A^2/4B along with the times tested in this work. Conventional processes (425C/10-60s) are all strongly diffusion limited.

1) B.E. Deal , A.S. Grove, *J. Appl. Phys.* **36**, 3770 (1965)
2) F.M. d'Heurle , *J. Mater. Res.* **3**, 167 (1988)

Fig. 1: Conductivity higher on poly than active. For Cond'ty above 0.15, all Co was consumed, so does not fit trend lines.

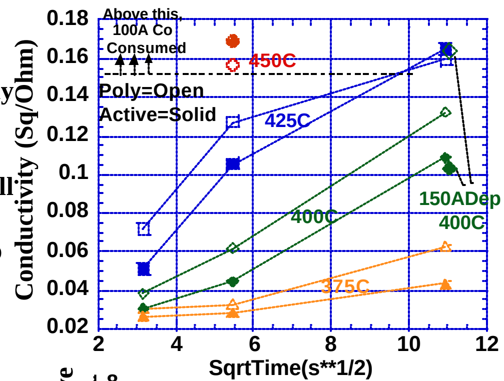

Fig. 2: CoSi2 thickness ratio (Poly/ Active). For intermediate temps & times, a maximum is reached.

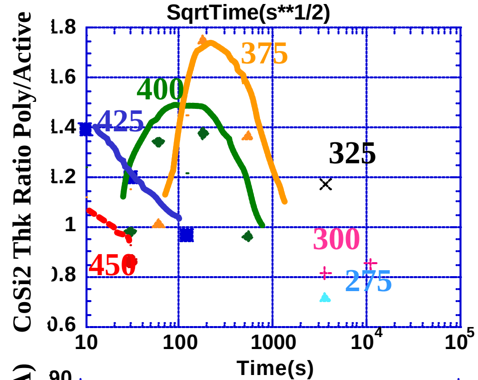

Fig. 3: Plotting Thickness-vs-Time/ Thickness provides good fits to Deal-Grove model.

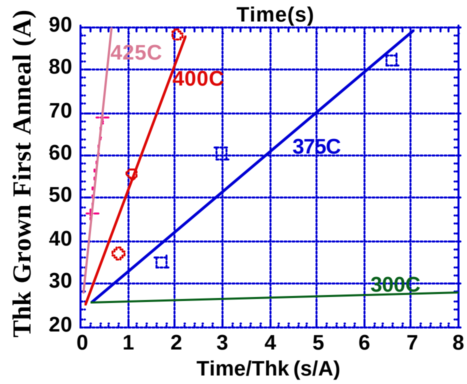

Fig. 4: Slopes from Fig. 3 give parabolic rate constant 'B'. Poly and mono silicon give very similar activation energies.

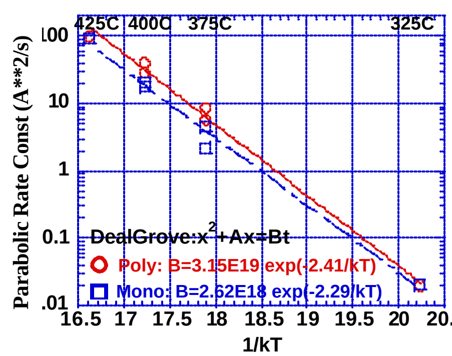

Fig. 5: Data points are A²/4B. Bars are the times used in this work. High temps were diff'n limited.