

## HIGH-VOLTAGE CMOS AND SCALING TRENDS

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The continuous increase of transistor density in ULSI integrated circuits (IC) drives the decrease of the maximum supply voltage in modern CMOS technologies. While such technologies are optimized for higher speed and lower power consumption, they cannot serve applications where high-voltage capabilities are required.

High-voltage technologies are dedicated to fill this gap by combining low-voltage and high-voltage features on the same substrate, at the expense of a lower integration density. Different combinations are possible depending on the application requirements in terms of voltage and current ratings. High-voltage CMOS technologies are widely used in applications such as flat panel displays where the voltage range is between 10V and 100V but the current is low. Smart Power and BCD (Bipolar, CMOS and DMOS) technologies are more dedicated for power applications with high currents such as motor drivers. This paper focuses on the architecture and scaling of high-voltage CMOS technologies for flat panel Liquid Crystal Display (LCD) drivers.

High-voltage CMOS can implement either Double Diffused Drain MOS (DDDMOS) or Lateral Drain MOS (LDMOS) devices, for voltages below 20V and 100V respectively. The low voltage part in both cases uses standard sub-micron CMOS transistors. The cross sections shown in Figure 1 and Figure 2 represent typical high-voltage CMOS process architectures used in active and passive matrix LCD displays. The key scaling parameters for a high integration density are also pointed out for each process.

The DDDMOS process architecture is typically used for column drivers in active matrix LCD displays, where a maximum transistor density is required particularly in the high-voltage part. In fact, the column driver is a high-voltage D/A converter where the low-voltage input digital code selects one of  $2^{n+1}$  high-voltage output grayscale levels per pixel. Thus, 80% of the chip area is dedicated for the multiplexer and the analog output buffer. The critical parameters at the transistor level to optimize the area efficiency are the drain extension  $L_d$ , the drift extension  $L_x$  and the channel length  $L_c$ . At the process backend level, the number of metal layers as a function of the grayscale levels is an important parameter.

The LDMOS process architecture is typically used for the row drivers in active matrix LCD displays and common drivers in passive matrix displays. In these ICs the function is a simple high-voltage shift register activating the selected row of the matrix. In this case the ratio between high-voltage and low-voltage parts is even higher than in the column driver. Thus, the critical parameters at the transistor level remain unchanged except that in LDMOS, additional guard rings are required between high-voltage devices due to the higher voltage value. Consequently, the minimum distance  $dx$  between the drain and the guard ring is also a dominant factor in the scaling.

Finally, the trend in high-voltage CMOS ICs is to add more complex low-voltage signal processing functions to meet the requirements of System On Chip (SoC) solutions. Typically, today's single chip display solutions used for handheld applications, implement the high-voltage drivers, a simple controller the memory, the

power supplies and the interface functions. Hence, the level of integration is also increasing, but is limited by the high-voltage features. Figure 3 shows the evolution of high-voltage CMOS technologies for the past 2 years. The minimum channel length applies for the low-voltage transistors.

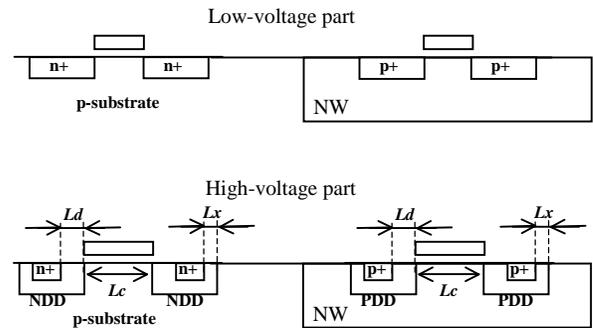


Figure 1: DDDMOS process architecture

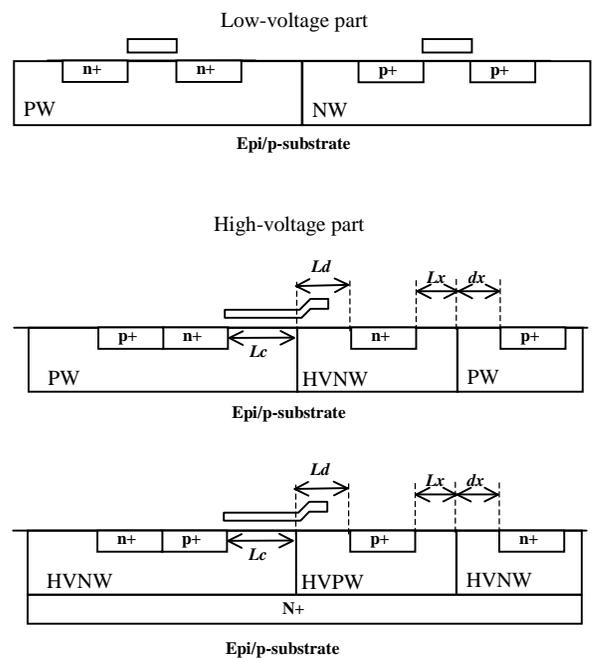


Figure 2: LDMOS process architecture

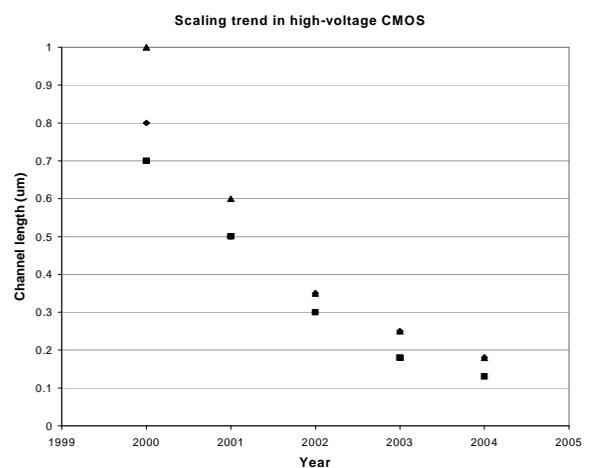


Figure 3: Scaling trend in high-voltage CMOS