Integration Issues with High k Gate Stacks

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Continued scaling of ULSI devices requires scaling of the equivalent oxide thickness (EOT) of the gate dielectric. However direct tunneling through ultra-thin oxides leads to unacceptable gate leakage currents, especially for low power applications. Thus alternative high k dielectrics are being sought to replace oxide and oxynitride as the gate dielectric. Furthermore metal gate electrodes are needed to eliminate dopant depletion effects in Poly-Si gates. Integration of these new materials into ULSI devices requires the development of new technologies and poses several new challenges. Conversely, the thermal processing associated with conventional integration schemes imposes severe constraints on the materials that can be used in gate stacks. This paper describes some of the key challenges and constraints and provides some examples of successful, as well as unsuccessful, integration.

The thermal budget associated with gate first integration schemes provides one of the most severe constraints on the high k dielectric. Unless a complex replacement-gate process is employed, the gate stack must withstand junction formation temperature cycles, which may range from 10's of seconds at 950ºC to spike anneals at 1050ºC to flash anneals at 1100ºC to pulsed laser annealing near the melting point of Si. Under these conditions: i) Hf and Zr oxides crystallize, ii) their silicates can phase separate, iii) La and Y oxides react with interfacial SiO_2 to form lower-k silicates as well as an electrically degraded interface, and iv) depending on the partial pressure of oxygen in the annealing atmosphere, the oxide can either be reduced, leading to silicide formation at the Si substrate or Poly-Si gate, or additional oxide can be grown, leading to higher and less-controllable EOT. Thus thermal budget considerations lead to the need for thermally-stabilized dielectrics, which may be achieved through nitridation or alloying with Al_2O_3.

The stability of EOT during subsequent annealing is of key concern in integration. Dielectrics containing OH in their bulk (e.g., from incomplete dissociation of MO precursors) or adsorbed water on the (porous?) surface are susceptible to the growth of additional oxide and poor EOT control. Alternate techniques have been explored to reduce this sensitivity: i) in-situ annealing after high k deposition to drive out residual OH and to densify the films, ii) nitridation of the bottom interface, top surface, or bulk of the high k to prevent additional oxidation of the substrate or transport of oxidants to the interface, and iii) in-situ gate deposition (or capping).

Gate electrodes provide several additional integration concerns. On the one hand, there is considerable experience with using Poly-Si and it seems unlikely that manufacturers will want to simultaneously switch both dielectric and gate electrode materials. Thus it seems likely that the introduction of high k dielectrics will be in conjunction with Poly Si (or Poly SiGe) gates. On the other hand Poly-Si gates add about 0.3 nm to the capacitance equivalent thickness (CET) and provide a source of boron, which penetrates most of the simple, high-k oxides. Minimization of short channel effects, at least in bulk CMOS, requires dual workfunction gate electrodes. The integration of two separate gate materials, one for NMOS and one for PMOS, likely requires the deposition of two separate gate dielectrics, since etching the first gate electrode is expected to damage the surface of any remaining dielectric, making it unsuitable for the other gate electrode material. Thus, to simplify the overall process, it is highly desirable to identify a suitable gate electrode system, i.e., one in which the workfunction can be locally tuned after blanket gate deposition. Proposed schemes to accomplish this include ion implantation (e.g. N into Mo) or alloying (e.g., Ta into Ru). Of course, the use of any alternate gate electrode material (or clad materials) requires the development of new, selective RIE processes, which meet the ITRS requirements on gate electrode dimensional control.

Successful integration of high-k gate stacks also requires attention to other processes such as optimization of post-deposition and post metallization anneals. Just as with the Si/SiO_2 system, high k gate stacks (at least those having oxide interfacial layers) benefit from forming gas anneals, which reduce interface state densities and improve channel mobilities. Deuterium has been show to be superior to hydrogen for annealing. However, the optimal annealing temperature for several high-k gate stack systems has been shown to be higher than that for Si/SiO_2.

In spite of the attention paid to these integration issues by the worldwide research community, the results to date have been mixed. While a number of material systems meet many of the individual criteria (e.g., gate leakage) for high k gate stacks, none of them has yet been demonstrated to simultaneously meet all the criteria. Achieving high drive current has been a persistent problem in devices. Especially those having very low EOTs. This low drive has been ascribed either to charges within the high k which scatter carriers in the channel or to centers which trap, and thereby reduce, channel charge. Devices are also susceptible to shifts in threshold voltage and transconductance as a result of stressing. However, we have observed room temperature recovery of these shifts, so that their long-term impact may be manageable.

Despite the somewhat mixed results with fully integrated devices, considerable progress has occurred over the past few years. Many material systems have been eliminated from further consideration, and the limitations of others have been quantified. The scientific understanding of the electronic structure and thermal properties of these materials, gained over the course of this work, is leading to a convergence on a rather limited set of materials and processes to make them. Thus there is considerable optimism that the materials and processes for commercialization will soon be at hand.