Abstract No. 981

Analysis of CMOS gate-to-drain leakage current and Proposition of a New Cobalt Salicide Selective Etch Chemistry for high DRAM yield.

Benoît Froment, Christophe Régnier, Marie-Thérèse Basso

STMicroelectronics
850 rue Jean Monnet, 38926 Crolles, France

A new efficient method of post-silicide formation wet strip has been developed. Based on SC1-SC2 combination, the recipe allows a decrease in cobalt salicide sheet resistance, the suppressing of the gate to drain leakage current (bridging), and contribute to a significant increase in circuit yield.
It is also shown that the bridging issue can come from at least three causes: CoSi residues left on the nitride spacer, cobalt atoms that diffuse during RTA1 in the first tens angstroms and that are not completely cleaned, and cobalt-based precipitates created if the wet etch process ends by an alkaline chemistry.

The traditional form of cobalt self-aligned salicide processing often involves a single wet chemical process aimed at removing the un-reacted metal from the STI isolation and the sidewall spacer, silicide filaments, and leaves the moat/gate salicide mostly untouched. However as CMOS dimensions shrink, the salicide thickness shrink also, and the minimum CoSi have to be etched during selective etch. That is why 2-steps chemistries dilute-HF-based [1,2] becomes obsolete, since they lead to high CoSi thickness etch, to a narrow process window (more detail in extended paper) and do not remove particles contamination.

A new approach has to be considered and detailed causes of bridging have to be investigated more in details. The first part makes a status on the main process causes creating bridging. The second one deals with the development an improved recipe called HOTSC2–SC1–SC2. Electrical, yield, and morphological aspects are discussed in the last part.

The salicide process used for cobalt is the following: a 200Å HF desoxidation followed by a 10Å Ar^+ Soft Sputter Etch (SSE), 80Å Co deposition with a 100Å TiN-capping layer. Then a RTP1 530°C 30s transforms Co into CoSi, the selective etch removes the un-reacted Co, then a RTA2 transforms CoSi into CoSi2.

We will show more in details in the extended paper that the bridging effect comes mainly from 3 origins as summarized in Fig.1:
1) CoSi residues formed from the Si atoms sputterized from the active region to the spacer by the 10Å SSE.
2) The Co atoms deposited on spacer diffuse into the nitride during RTA1 and remain unstripped.
3) The cobalt-based precipitates created during the alkaline SC1 chemistry can limit the nitride etch by remaining on spacer, especially if they are not solubilized by a following acidic solution (SC2 for example). The selective etch have to end by an acidic solution.

In order to characterize each selective etch recipe step (etch rate of all materials at play and Co residues quantification) full sheet wafers have been prepared. The Co 80Å/TiN 100Å stack has been deposited and annealed on thermal oxide (to simulate STI), on nitride (to simulate the spacer), on TEOS, and on bare silicon. Then TXRF has been performed on oxide and nitride wafers after selective etch. The equivalent oxide, TEOS and nitride thickness etched were monitored by opti-probe measurement on dedicated full sheet wafers.

As described in [1,2] the use of acidic SC2 allows the Co strip to be nearly simultaneous with TiN removal. The Co etch rate in a hot (65°C, 1:1:10) SC2 is so much higher than the TiN etch rate that the Co is essentially gone as soon as the TiN clears. Then it is necessary to have a controlled etch of the nitride spacer in order to remove filaments, CoSi and Co aggregates present on the sidewalls. Therefore a SC1 chemistry (65°C, 1:2:10) is required since the nitride and CoSi etch rate is relatively moderated. But finishing by a SC1 step could let cobalt composite residues on the spacer that could creates leakage. Indeed, in SC2 and DI water Co is present in the form of Co^{2+}, whereas in SC1 solutions, Co should be present as $Co(NH3)_6^{2+}$, Co_3O_4 or $Co(OH)_2$ species depending on pH values of solutions (Pourbaix diagram) [3]. Therefore an acidic cold SC2 have been used to end the recipe, followed by a hot rinse in DI to decrease metallic contamination.

The TXRF contamination data were 1.33e12 Co at/cm² on oxide, 8e12 Co at/cm² on nitride, and oxide, nitride and CoSi thickness etched were respectively 4.5Å, 2Å, and 14Å (small compared to 300Å total silicide thickness). Various morphological and electrical measurement results will be discussed at the conference: morphological SEM aspect was improved, active and poly resistance decreased, gate to drain current leakage was completely suppressed, and DRAM yield, very sensitive to defectivity and leakage, increased significantly.

REFERENCES
1. S. O'Brien, ECS Proc. V97-35, p579
2. M.R. Baklanov, et al, J. Electrochem. Soc. 143(10) p.3245 (1996)
3. Joong S. Jeon, ECS Proc., V99-36, p.150.

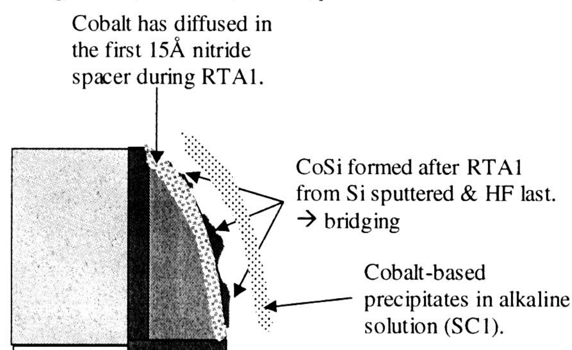

Fig. 1 Different Co-residues that may affect bridging leakage. Cross-section of a nitride spacer after a not optimised selective etch (exemple: SC1-SC2 (cold)).