An Analysis of the Effect of the Steps for Isolation Formation on STI Process Integration

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Introduction

While device dimensions are scaled down the shallow trench isolation (STI) technology could face with reliability problems related to the impact on electrical behavior of the morphology of the region neighboring active area. Gate wraparound of the trench corner and active oxide thinning can cause a hump in the transistor Id-Vg characteristic [1] and a parasitic conduction with degradation in oxide reliability. Aim of this work is to investigate process parameters that influence this anomalous behavior in order to prevent process integration problems from occurring while setting up a new process flow.

Experimental Results and Simulation Analysis

The STI is formed by the growth of a thermal pad-oxide and the deposition of a nitride layer. A shallow trench, masked with stacked photo resist/nitride/oxide layers, is etched. After photo resist strip a liner oxide is grown. This oxidation, eventually combined with a pad oxide undercut, can achieve a good rounding of the active area corner and remove the damage caused by the trench etching [2]. The trench is then filled by HDP or TEOS-CVD oxide which is polished down by CMP to expose the top of the nitride, which is then removed by a wet etch. Wells are then formed by ion implantation, followed by residual oxide removal and active oxide growth. It is known that the Qbd of the active oxide is improved by the use of a dummy oxide [3] grown after nitride removal. Historically this dummy oxide was introduced to prevent the Kooi effect in LOCOS isolation scheme, and it is supposed to reduce also the process related stress [5]. To perform our investigation large area capacitors as well as edge intensive structures on both n- and p- substrate were used.

Looking at the TEM cross section of an active area edge (fig.1 left) obtained using a non-optimized process, we observe a variation of active oxide thickness, due to different surface orientation and stress condition [6]. Moving from the active area center to the corner there is a gradual increase of oxide thickness, followed by a local thinning, just where the poly wraps around the trench corner. We have analyzed many technological items that can be varied in order to modify the oxide thickness variation leading to anomalous electrical characteristics, such as for instance liner oxidation process that we found to have a low impact on this STI scheme. We focused our attention on the role played by dummy oxide and on the effect of the wet etch used to remove the residual oxide before the active oxide growth, directly related to poly wraparound and hump effect [7].

In fig.1 – right side - a TEM cross section of an active area corner obtained with an optimized process is shown. Oxide thinning is reduced; silicon profile is smoother and the double slope observed in fig.1 is absent. Moreover, it is also possible to notice a different rounding of the poly/oxide interface that is evaluated by a varied curvature radius. To achieve this, dummy oxide proved to be a sensitive element. The improvements were obtained only by changing the type of oxidation from a low thermal budget (non-optimized) to a high thermal budget one (optimized). Temperature, time and process ambient were taken into account. High thermal budget processes seem to be more effective in modifying the Si profile during the oxidation and in relaxing the stress. Among the various parameters compared in high and low thermal budget processes, oxide thickness seems to be the less important.

Another parameter we investigated was the wet etching performed before the active oxide growth. To remove the residual oxide, we use a commercial diluted BOE solution ($NH_4F/HF/H_2O$) and in our experiment we varied the over etch on active area from 0% to 80% with respect to the oxide thickness measurement. We expected a variation in poly wraparound as well as a possible modification of poly-oxide interface profile due to the different etching amounts.

For a non-optimized process the double effect of thinning and rounding of poly-oxide interface is present, as confirmed by the great difference observed between the J(V) characteristics of area and periphery devices. The asymmetry between J(V) characteristics for negative and positive gate voltage can be explained by an anomalous rounding of poly/oxide interface, already pointed out in morphological analysis. A tunneling current simulation on a simplified structure is represented in fig.2 (inlet): a first region has a uniform oxide thickness and flat-gate silicon, the second a thinner oxide with the curvature radius representing the variable poly/oxide interface shape (values for simulations are derived from TEM sections). A good agreement is found between experimental data and current simulation for edge intensive capacitors, as shown in fig. 2. In fig. 3 we show the voltage necessary to sustain an injection of 1E-5A/cm2 (Vin) for low and high thermal budget process: a significant improvement is evident for both positive and negative injection polarity increasing the dummy oxide thermal budget, while the simple increase of oxidation thickness is not effective. In fig. 4, the impact of BOE etches is reported: as expected an increase of over etch worsens the poly silicon wrap around causing a lower Vin on peripheral capacitors.

Conclusions

In order to set up a robust STI process and to prevent possible integration problems, an extensive analysis was carried out regarding the effects of STI steps on process reliability. For the STI analyzed process sequence dummy oxide and wet etch before active oxide growth proved the most effective issues. A process sequence characterized by high thermal budget dummy oxide and a reduced BOE etch was found to achieve the best morphological and electrical results on elementary test structures.

References

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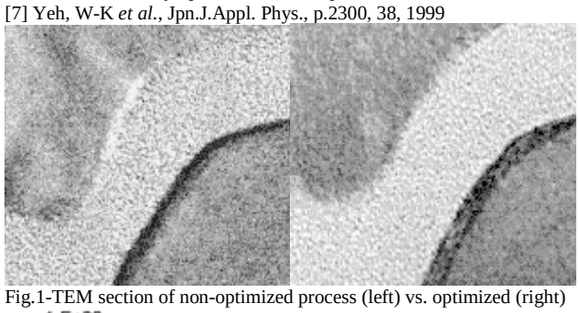

Fig.1-TEM section of non-optimized process (left) vs. optimized (right)

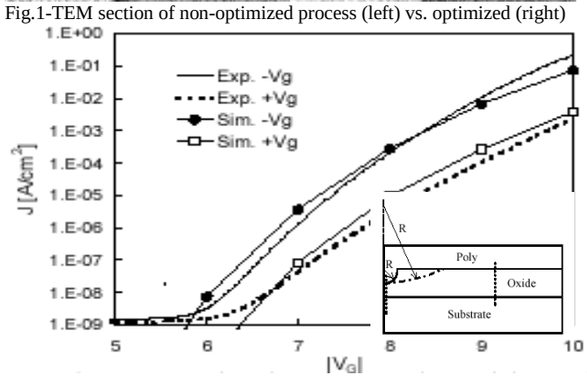

Fig. 2 – J-V characteristics - experimental and simulations (peripheral capacitors).

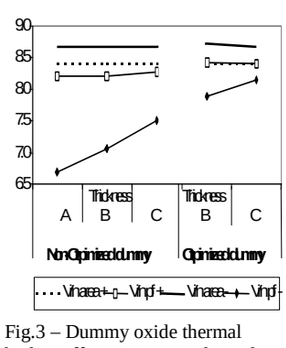

Fig.3 – Dummy oxide thermal budget effect on gate oxide quality

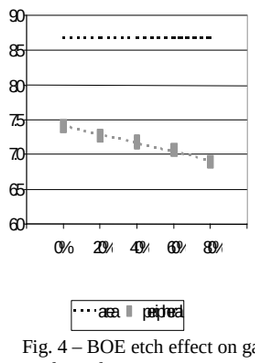

Fig. 4 – BOE etch effect on gate oxide quality