Defect generation and suppression in device processes using a Shallow Trench Isolation scheme

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Recently it was pointed out that crystal defects are very harmful in present silicon devices when responsible for a source-to-drain junction piping and hence for a transistor leakage current. Defect formation is very often related to the isolation technology as process steps responsible for the development of relevant stress in silicon. This effect becomes more and more important with shrinking device size and it is dramatic when the Shallow Trench Isolation (STI) technology is used. The pattern geometry is found to be a key issue in defect formation and the role of active area corners is evident both in experiments and in numerical simulations.

Specific test structures, consisting of transistor array with minimum gate length and a high density of active area corners, were drawn to reproduce a critical pattern for defect formation and activation.

In this paper the critical factors for defect formation are identified and various approaches to the problem of defect suppression in device processing are discussed. The mechanical elastic stress is of course critical for defect formation. The mechanisms of stress development are identified by comparing experimental results and numerical simulations, and the evolution of the elastic stress during the process is studied by measurements of the Raman shift. Thermal oxidations of the STI structure are reported to be a major responsible of the stress increase. The problem of process optimization from the point of view of mechanical stress reduction is then addressed. For instance, it is shown that modifications of the oxidation technology may result in an important stress reduction (see fig. 1).. This result is also confirmed by numerical simulations, however the available models show some limitations in describing the stress evolution in the process. In addition, it is found that the stress developed at the active area edge can be reduced by modifying the isolation structure. A short etching of the isolation oxide was found to be beneficial in reducing both the elastic stress in the process as obtained by RAMAN shift measurements (fig. 2) and the leakage current of our test structures. This fact is confirmed by numerical calculation of the stress in silicon, showing that the stress component responsible for defect generation is reduced by such etching.

Implantation conditions and implantation damage recovery result to be another key factor in defect generation. Ion implantation may concur to defect generation because of both point defect injection and defect nuclei formation. Specifically, the recristallization of a highly stressed region is found to be the step where defects are most frequently generated. Indeed, defects most frequently appear in or close to regions receiving arsenic implantations at doses well above the amorphization dose. Vice versa, room temperature high dose boron implantations do not produce an amorphous layer, and in fact these implantations do not generally induce defect formation. However defect formation and the related transistor leakage can be activated by a pre-amorphizing silicon implantation before the boron implantation. For what concerns the optimization of the implantation process, it is found that an energy reduction of any arsenic high dose implantation is beneficial, possibly because end-of-range defects are more easily annealed out if they are located close to wafer surface. A modification of the implantation screen oxide, though with the same projected range in silicon, is also found to be beneficial in reducing transistor array leakage current. However, TEM inspections of the amorphous layer show that different screen oxides produce amorphous layers with a different shape in the active area corner, i.e. in the region where mechanical stress is maximum. It is suggested that the amorphization of the highly stressed region reduces the energy barrier for defect formation, so defects are more easily generated during the recristallization of an amorphous layer.

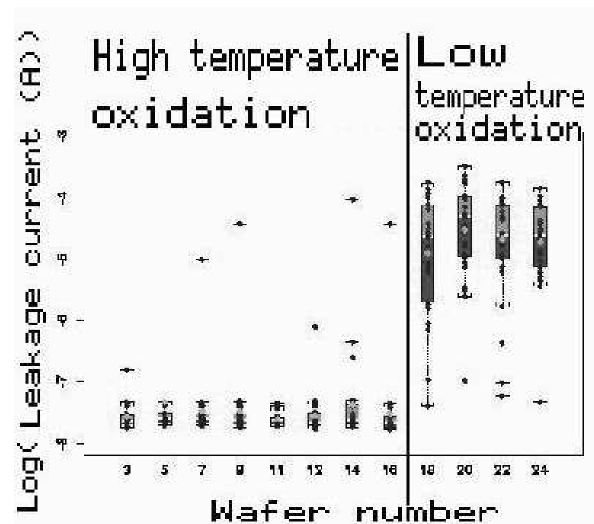

Fig. 1. Transistor array leakage current vs. oxidation technology

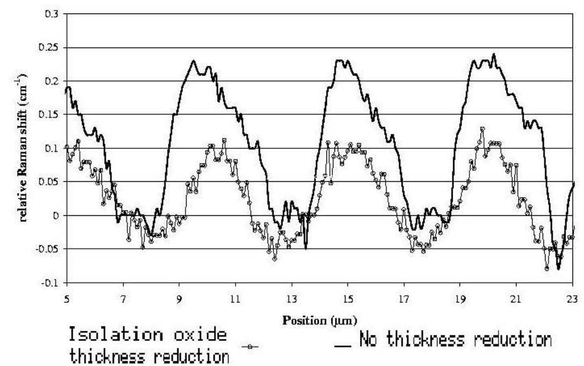

Fig. 2. Raman shift measurements in samples with different isolation oxide thickness